

Model Name : H510M H

Rev 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1150-D
08	DDR4 CHANNEL A
09	DDR4 CHANNEL B
10	PCH_CLK BUFFER
11	PCH_DMI,USB,PCIE
12	PCH_MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR
15	PCH GND
16	ITE 8686 LPC IO
17	HWM
18	FAN CTRL--SIO
19	BIOS
20	CEC
21	PCI EXPRESS*16 SLOT
22	PCI EXPRESS*1 SLOT
23	SATA Connector
24	M.2 X4 (A)
25	IT8892E (NA)
26	PCI SLOT (NA)
27	ASM1085 POWER (NA)
28	LDO POWER (NA)

SHEET

TITLE

29	ISL95866 PWM-IRON
30	ISL95866 VCORE-IRON
31	ISL95866 VCCGT-IRON
32	VCCSA_VCCIO_VCCPLL
33	RT8237_DDR_BEAD
34	RT8068A_VPP
35	RT8237_PCH-BEAD
36	DISCRETE POWER
37	POWER MAP
38	ATX POWER , A_-PROCHOT
39	KB_MS
40	DVI CONN
41	RTD2168 - DP to VGA - IC
42	RTD2168 - DP to VGA - Conn
43	REALTEK 8111G
44	USB_LAN CONNECTOR-81118
45	Realtek ALC887
46	REAR AUDIO JACK
47	ADUIO LED
48	R_USB30_1
49	R_USB30_2
50	HDMI (MASK)
51	Redriver-R_USB31 (NA)
52	F_USB30
53	F_USB
54	F_PANEL
55	COM, TPM
56	EMI-ESD
	NTC MAP

Gigabyte Technology

Title			Cover Sheet
Size	Document Number	H510M H	
Custom			Rev 1.0
Date:	Wednesday, January 06, 2021	Sheet 1	of 62

Model Name : H410M H

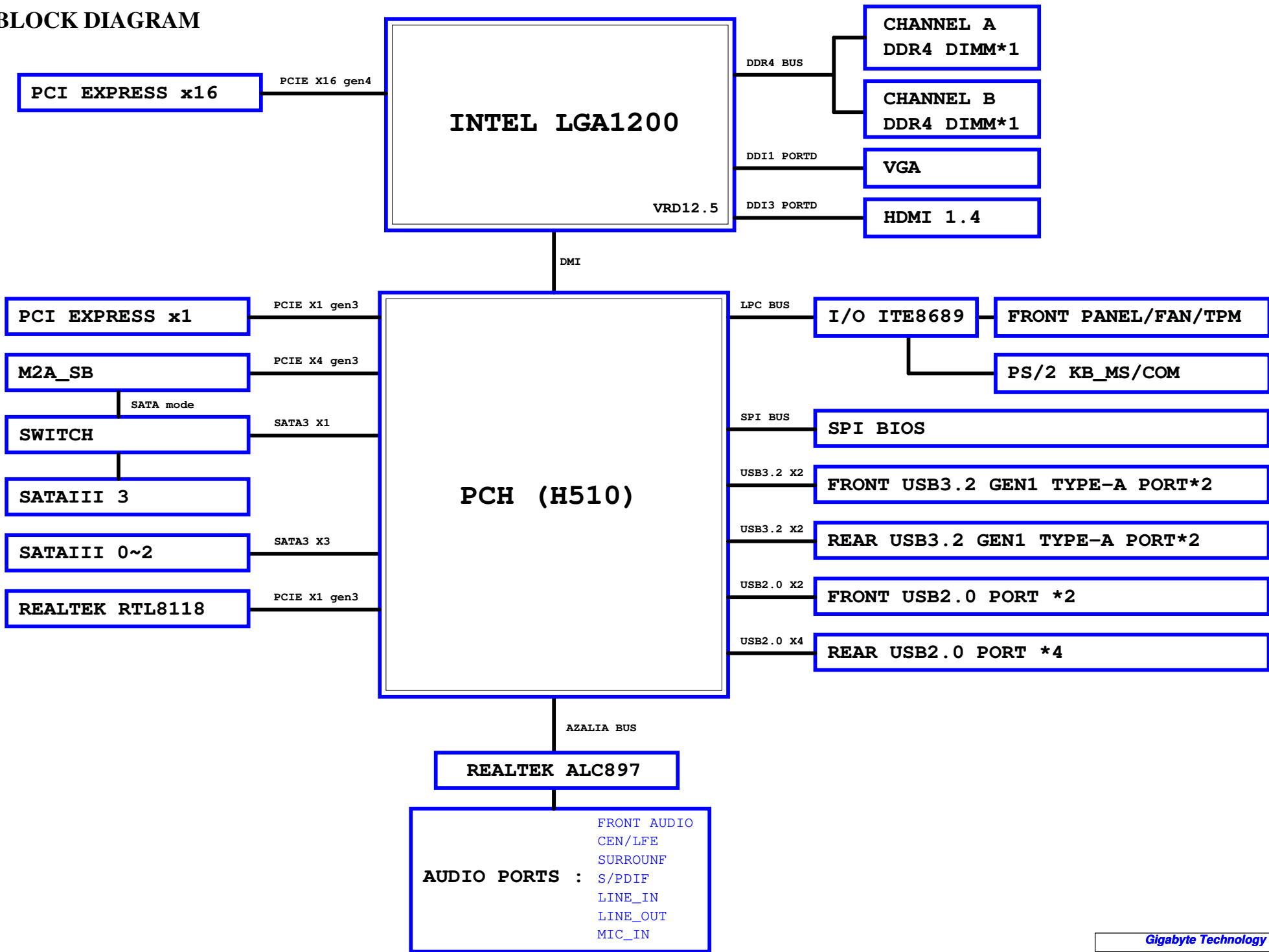
Component value change history

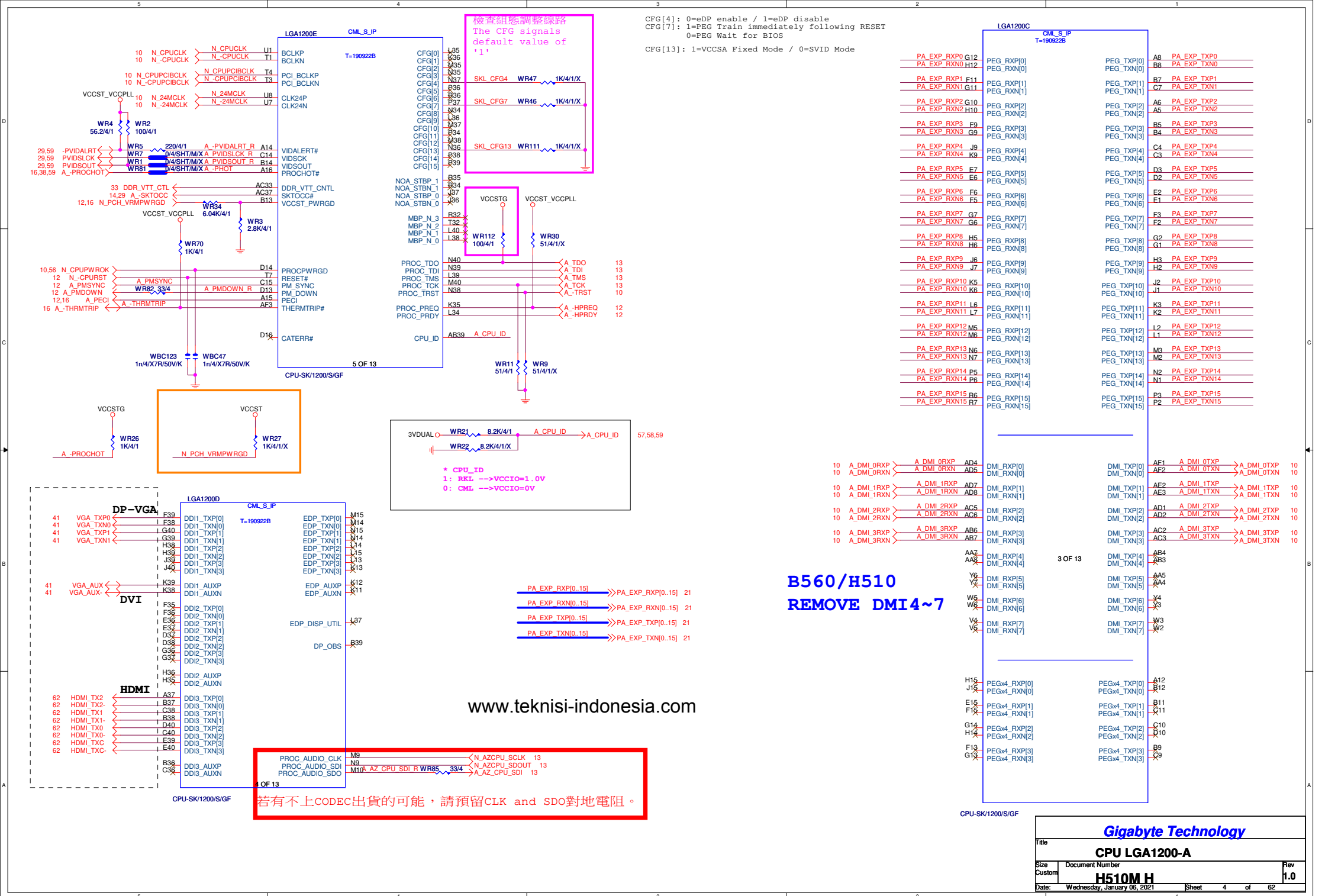
Data	Change Item	Reason
2019/12/12	1. H410M H 改 S2	R01
2019/12/12	1. EVT	9MH410MS2-00-01
2020/02/24	1. 修改模組線路 & note	R10
2020/03/12	1. DVT	9MH410MS2-00-10A
2020/03/17	1. 修改模組線路 & note	R101
2020/03/29	1. PVT	9MH410MS2-00-10E
2020/04/07	1. 修改模組線路 & note	9MH410MS2-00-10F
2020/04/17	1. 採購修改電容用料	9MH410MS2-00-10G
2020/08/27	1. H410M S2 改 H510M S2	R01

Circuit or PCB layout change

DATE	Change Item	Reason

BLOCK DIAGRAM





## LGA1200A

## CML\_S\_IP

T-190922B

MDA0 AE39	DDR0_DQ[0]	DDR0_CKP[0]	AW24 M_DCLKA0	DDR0_CKP[0]	AW24 M_DCLKA0	8
MDA1 AE38	DDR0_DQ[1]	DDR0_CKN[0]	AW23 M_DCLKA1	DDR0_CKN[0]	AW23 M_DCLKA1	8
MDA2 AH39	DDR0_DQ[2]	DDR0_CKP[1]	AW23 M_DCLKA1	DDR0_CKP[1]	AW23 M_DCLKA1	8
MDA3 AH38	DDR0_DQ[3]	DDR0_CKN[1]	AW23 M_DCLKA1	DDR0_CKN[1]	AW23 M_DCLKA1	8
MDA4 AF40	DDR0_DQ[4]	DDR0_CKP[2]	AW19 M_DCLKA1	DDR0_CKP[2]	AW19 M_DCLKA1	8
MDA5 AE40	DDR0_DQ[5]	DDR0_CKN[2]	AW18 M_DCLKA1	DDR0_CKN[2]	AW18 M_DCLKA1	8
MDA6 AH40	DDR0_DQ[6]	DDR0_CKP[3]	AW18 M_DCLKA1	DDR0_CKP[3]	AW18 M_DCLKA1	8
MDA7 AG40	DDR0_DQ[7]	DDR0_CKN[3]	AW18 M_DCLKA1	DDR0_CKN[3]	AW18 M_DCLKA1	8
MDA8 AK39	DDR0_DQ[8]	DDR0_CKE[0]	AW31 CKEA0	DDR0_CKE[0]	AW31 CKEA0	8
MDA9 AK40	DDR0_DQ[9]	DDR0_CKE[1]	AW31 CKEA1	DDR0_CKE[1]	AW31 CKEA1	8
MDA10 AN39	DDR0_DQ[10]	DDR0_CKE[2]	AW31 CKEA1	DDR0_CKE[2]	AW31 CKEA1	8
MDA11 AM40	DDR0_DQ[11]	DDR0_CKE[3]	AW31 CKEA1	DDR0_CKE[3]	AW31 CKEA1	8
MDA12 AL40	DDR0_DQ[12]	DDR0_CS#0	AW15 M_CSA0	DDR0_CS#0	AW15 M_CSA0	8
MDA13 AK38	DDR0_DQ[13]	DDR0_CS#1	AW13 M_CSA1	DDR0_CS#1	AW13 M_CSA1	8
MDA14 AN40	DDR0_DQ[14]	DDR0_CS#2	AW13 M_CSA1	DDR0_CS#2	AW13 M_CSA1	8
MDA15 AN38	DDR0_DQ[15]	DDR0_CS#3	AW13 M_CSA1	DDR0_CS#3	AW13 M_CSA1	8
MDA16 AR39	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_ODT0	AW14 MODT_A0	DDR0_ODT0	AW14 MODT_A0	8
MDA17 AR40	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_ODT1	AW14 MODT_A1	DDR0_ODT1	AW14 MODT_A1	8
MDA18 AV39	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_ODT2	AW14 MODT_A1	DDR0_ODT2	AW14 MODT_A1	8
MDA19 AL40	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_ODT3	AW14 MODT_A1	DDR0_ODT3	AW14 MODT_A1	8
MDA20 AR38	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_ODT4	AW14 MODT_A1	DDR0_ODT4	AW14 MODT_A1	8
MDA21 AT40	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_ODT5	AW14 MODT_A1	DDR0_ODT5	AW14 MODT_A1	8
MDA22 AV38	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_ODT6	AW14 MODT_A1	DDR0_ODT6	AW14 MODT_A1	8
MDA23 AV38	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_ODT7	AW14 MODT_A1	DDR0_ODT7	AW14 MODT_A1	8
MDA24 AV36	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_ODT8	AW14 MODT_A1	DDR0_ODT8	AW14 MODT_A1	8
MDA25 AV36	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_ODT9	AW14 MODT_A1	DDR0_ODT9	AW14 MODT_A1	8
MDA26 AV33	DDR0_DQ[26]/DDR0_DQ[42]	DDR0_ODT10	AW14 MODT_A1	DDR0_ODT10	AW14 MODT_A1	8
MDA27 AV34	DDR0_DQ[27]/DDR0_DQ[43]	DDR0_ODT11	AW14 MODT_A1	DDR0_ODT11	AW14 MODT_A1	8
MDA28 AV35	DDR0_DQ[28]/DDR0_DQ[44]	DDR0_ODT12	AW14 MODT_A1	DDR0_ODT12	AW14 MODT_A1	8
MDA29 AV36	DDR0_DQ[29]/DDR0_DQ[45]	DDR0_ODT13	AW14 MODT_A1	DDR0_ODT13	AW14 MODT_A1	8
MDA30 AY33	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_ODT14	AW14 MODT_A1	DDR0_ODT14	AW14 MODT_A1	8
MDA31 AW33	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_ODT15	AW14 MODT_A1	DDR0_ODT15	AW14 MODT_A1	8
MDA32 AW11	DDR0_DQ[32]/DDR0_DQ[0]	DDR0_ODT16	AW14 MODT_A1	DDR0_ODT16	AW14 MODT_A1	8
MDA33 AV11	DDR0_DQ[33]/DDR0_DQ[1]	DDR0_ODT17	AW14 MODT_A1	DDR0_ODT17	AW14 MODT_A1	8
MDA34 AV7	DDR0_DQ[34]/DDR0_DQ[2]	DDR0_ODT18	AW14 MODT_A1	DDR0_ODT18	AW14 MODT_A1	8
MDA35 AY8	DDR0_DQ[35]/DDR0_DQ[3]	DDR0_ODT19	AW14 MODT_A1	DDR0_ODT19	AW14 MODT_A1	8
MDA36 AW9	DDR0_DQ[36]/DDR0_DQ[4]	DDR0_ODT20	AW14 MODT_A1	DDR0_ODT20	AW14 MODT_A1	8
MDA37 AW10	DDR0_DQ[37]/DDR0_DQ[5]	DDR0_ODT21	AW14 MODT_A1	DDR0_ODT21	AW14 MODT_A1	8
MDA38 AV7	DDR0_DQ[38]/DDR0_DQ[6]	DDR0_ODT22	AW14 MODT_A1	DDR0_ODT22	AW14 MODT_A1	8
MDA39 AW7	DDR0_DQ[39]/DDR0_DQ[7]	DDR0_ODT23	AW14 MODT_A1	DDR0_ODT23	AW14 MODT_A1	8
MDA40 AW5	DDR0_DQ[40]/DDR0_DQ[8]	DDR0_ODT24	AW14 MODT_A1	DDR0_ODT24	AW14 MODT_A1	8
MDA41 AV5	DDR0_DQ[41]/DDR0_DQ[9]	DDR0_ODT25	AW14 MODT_A1	DDR0_ODT25	AW14 MODT_A1	8
MDA42 AW2	DDR0_DQ[42]/DDR0_DQ[10]	DDR0_ODT26	AW14 MODT_A1	DDR0_ODT26	AW14 MODT_A1	8
MDA43 AW3	DDR0_DQ[43]/DDR0_DQ[11]	DDR0_ODT27	AW14 MODT_A1	DDR0_ODT27	AW14 MODT_A1	8
MDA44 AV4	DDR0_DQ[44]/DDR0_DQ[12]	DDR0_ODT28	AW14 MODT_A1	DDR0_ODT28	AW14 MODT_A1	8
MDA45 AV5	DDR0_DQ[45]/DDR0_DQ[13]	DDR0_ODT29	AW14 MODT_A1	DDR0_ODT29	AW14 MODT_A1	8
MDA46 AV1	DDR0_DQ[46]/DDR0_DQ[14]	DDR0_ODT30	AW14 MODT_A1	DDR0_ODT30	AW14 MODT_A1	8
MDA47 AV2	DDR0_DQ[47]/DDR0_DQ[15]	DDR0_ODT31	AW14 MODT_A1	DDR0_ODT31	AW14 MODT_A1	8
MDA48 AT1	DDR0_DQ[48]/DDR0_DQ[16]	DDR0_ODT32	AW14 MODT_A1	DDR0_ODT32	AW14 MODT_A1	8
MDA49 AN1	DDR0_DQ[49]/DDR0_DQ[17]	DDR0_ODT33	AW14 MODT_A1	DDR0_ODT33	AW14 MODT_A1	8
MDA50 AT3	DDR0_DQ[50]/DDR0_DQ[18]	DDR0_ODT34	AW14 MODT_A1	DDR0_ODT34	AW14 MODT_A1	8
MDA51 AP1	DDR0_DQ[51]/DDR0_DQ[19]	DDR0_ODT35	AW14 MODT_A1	DDR0_ODT35	AW14 MODT_A1	8
MDA52 AT2	DDR0_DQ[52]/DDR0_DQ[20]	DDR0_ODT36	AW14 MODT_A1	DDR0_ODT36	AW14 MODT_A1	8
MDA53 AN3	DDR0_DQ[53]/DDR0_DQ[21]	DDR0_ODT37	AW14 MODT_A1	DDR0_ODT37	AW14 MODT_A1	8
MDA54 AR1	DDR0_DQ[54]/DDR0_DQ[22]	DDR0_ODT38	AW14 MODT_A1	DDR0_ODT38	AW14 MODT_A1	8
MDA55 AN2	DDR0_DQ[55]/DDR0_DQ[23]	DDR0_ODT39	AW14 MODT_A1	DDR0_ODT39	AW14 MODT_A1	8
MDA56 AL2	DDR0_DQ[56]/DDR0_DQ[24]	DDR0_ODT40	AW14 MODT_A1	DDR0_ODT40	AW14 MODT_A1	8
MDA57 AL3	DDR0_DQ[57]/DDR0_DQ[25]	DDR0_ODT41	AW14 MODT_A1	DDR0_ODT41	AW14 MODT_A1	8
MDA58 AL3	DDR0_DQ[58]/DDR0_DQ[26]	DDR0_ODT42	AW14 MODT_A1	DDR0_ODT42	AW14 MODT_A1	8
MDA59 AJ1	DDR0_DQ[59]/DDR0_DQ[27]	DDR0_ODT43	AW14 MODT_A1	DDR0_ODT43	AW14 MODT_A1	8
MDA60 AH3	DDR0_DQ[60]/DDR0_DQ[28]	DDR0_ODT44	AW14 MODT_A1	DDR0_ODT44	AW14 MODT_A1	8
MDA61 AL1	DDR0_DQ[61]/DDR0_DQ[29]	DDR0_ODT45	AW14 MODT_A1	DDR0_ODT45	AW14 MODT_A1	8
MDA62 AH2	DDR0_DQ[62]/DDR0_DQ[30]	DDR0_ODT46	AW14 MODT_A1	DDR0_ODT46	AW14 MODT_A1	8
MDA63 AK1	DDR0_DQ[63]/DDR0_DQ[31]	DDR0_ODT47	AW14 MODT_A1	DDR0_ODT47	AW14 MODT_A1	8

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CPU-SK/1200/S/GF

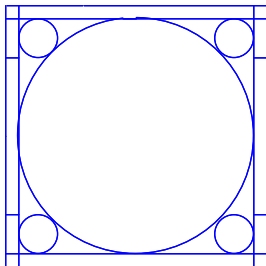
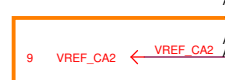
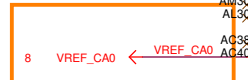
## CML\_S\_IP

T-190922B

MDB0 AD34	DDR1_DQ[0]/DDR0_DQ[16]	DDR1_CKP[0]	AW23 M_DCLKB0	DDR1_CKP[0]	AW23 M_DCLKB0	9
MDB1 AD35	DDR1_DQ[1]/DDR0_DQ[17]	DDR1_CKN[0]	AW22 M_DCLKB1	DDR1_CKN[0]	AW22 M_DCLKB1	9
MDB2 AE36	DDR1_DQ[2]/DDR0_DQ[18]	DDR1_CKP[1]	AW22 M_DCLKB1	DDR1_CKP[1]	AW22 M_DCLKB1	9
MDB3 AF36	DDR1_DQ[3]/DDR0_DQ[19]	DDR1_CKN[1]	AW22 M_DCLKB1	DDR1_CKN[1]	AW22 M_DCLKB1	9
MDB4 AG35	DDR1_DQ[4]/DDR0_DQ[20]	DDR1_CKP[2]	AW21 M_DCLKB1	DDR1_CKP[2]	AW21 M_DCLKB1	9
MDB5 AG34	DDR1_DQ[5]/DDR0_DQ[21]	DDR1_CKN[2]	AW21 M_DCLKB1	DDR1_CKN[2]	AW21 M_DCLKB1	9
MDB6 AD36	DDR1_DQ[6]/DDR0_DQ[22]	DDR1_CKP[3]	AW20 M_DCLKB1	DDR1_CKP[3]	AW20 M_DCLKB1	9
MDB7 AG36	DDR1_DQ[7]/DDR0_DQ[23]	DDR1_CKN[3]	AW20 M_DCLKB1	DDR1_CKN[3]	AW20 M_DCLKB1	9
MDB8 AJ36	DDR1_DQ[8]/DDR0_DQ[24]	DDR1_CKE[0]	AW25 CKEB0	DDR1_CKE[0]	AW25 CKEB0	9
MDB9 AJ35	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CKE[1]	AW26 CKEB1	DDR1_CKE[1]	AW26 CKEB1	9
MDB10 AL36	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CKE[2]	AW26 CKEB1	DDR1_CKE[2]	AW26 CKEB1	9
MDB11 AM35	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_CKE[3]	AW26 CKEB1	DDR1_CKE[3]	AW26 CKEB1	9
MDB12 AK36	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_CS#0	AW17 M_CSB0	DDR1_CS#0	AW17 M_CSB0	9
MDB13 AJ34	DDR1_DQ[13]/DDR0_DQ[29]	DDR1_CS#1	AW15 M_CSB1	DDR1_CS#1	AW15 M_CSB1	9
MDB14 AM36	DDR1_DQ[14]/DDR0_DQ[30]	DDR1_CS#2	AW15 M_CSB1	DDR1_CS#2	AW15 M_CSB1	9
MDB15 AM34	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_CS#3	AW15 M_CSB1	DDR1_CS#3	AW15 M_CSB1	9
MDB16 AT36	DDR1_DQ[16]/DDR0_DQ[32]	DDR1_ODT0	AW14 MODT_B0	DDR1_ODT0	AW14 MODT_B0	9
MDB17 AP36	DDR1_DQ[17]/DDR0_DQ[33]	DDR1_ODT1	AW14 MODT_B1	DDR1_ODT1	AW14 MODT_B1	9
MDB18 AT34	DDR1_DQ[18]/DDR0_DQ[34]	DDR1_ODT2	AW14 MODT_B1	DDR1_ODT2	AW14 MODT_B1	9
MDB19 AP33	DDR1_DQ[19]/DDR0_DQ[35]	DDR1_ODT3	AW14 MODT_B1	DDR1_ODT3	AW14 MODT_B1	9
MDB20 AR36	DDR1_DQ[20]/DDR0_DQ[36]	DDR1_ODT4	AW14 MODT_B1	DDR1_ODT4	AW14 MODT_B1	9
MDB21 AT35	DDR1_DQ[21]/DDR0_DQ[37]	DDR1_ODT5	AW14 MODT_B1	DDR1_ODT5	AW14 MODT_B1	9
MDB22 AR33	DDR1_DQ[22]/DDR0_DQ[38]	DDR1_ODT6	AW14 MODT_B1	DDR1_ODT6	AW14 MODT_B1	9
MDB23 AT33	DDR1_DQ[23]/DDR0_DQ[39]	DDR1_ODT7	AW14 MODT_B1	DDR1_ODT7	AW14 MODT_B1	9
MDB24 AP33	DDR1_DQ[24]/DDR0_DQ[40]	DDR1_ODT8	AW14 MODT_B1	DDR1_ODT8	AW14 MODT_B1	9
MDB25 AT31	DDR1_DQ[25]/DDR0_DQ[41]	DDR1_ODT9	AW14 MODT_B1	DDR1_ODT9	AW14 MODT_B1	9
MDB26 AT29	DDR1_DQ[26]/DDR0_DQ[42]	DDR1_ODT10	AW14 MODT_B1	DDR1_ODT10	AW14 MODT_B1	9
MDB27 AP28	DDR1_DQ[27]/DDR0_DQ[43]	DDR1_ODT11	AW14 MODT_B1	DDR1_ODT11	AW14 MODT_B1	9
MDB28 AR31	DDR1_DQ[28]/DDR0_DQ[44]	DDR1_ODT12	AW14 MODT_B1	DDR1_ODT12	AW14 MODT_B1	9
MDB29 AR31	DDR1_DQ[29]/DDR0_DQ[45]	DDR1_ODT13	AW14 MODT_B1	DDR1_ODT13	AW14 MODT_B1	9
MDB30 AB28	DDR1_DQ[30]/DDR0_DQ[46]	DDR1_ODT14	AW14 MODT_B1	DDR1_ODT14	AW14 MODT_B1	9
MDB31 AT28	DDR1_DQ[31]/DDR0_DQ[47]	DDR1_ODT15	AW14 MODT_B1	DDR1_ODT15	AW14 MODT_B1	9
MDB32 AT12	DDR1_DQ[32]/DDR0_DQ[0]	DDR1_ODT16	AW14 MODT_B1	DDR1_ODT16	AW14 MODT_B1	9
MDB33 AR12	DDR1_DQ[33]/DDR0_DQ[1]	DDR1_ODT17	AW14 MODT_B1	DDR1_ODT17	AW14 MODT_B1	9
MDB34 AT10	DDR1_DQ[34]/DDR0_DQ[2]	DDR1_ODT18	AW14 MODT_B1	DDR1_ODT18	AW14 MODT_B1	9
MDB35 AR10	DDR1_DQ[35]/DDR0_DQ[3]	DDR1_ODT19	AW14 MODT_B1	DDR1_ODT19	AW14 MODT_B1	9
MDB36 AP12	DDR1_DQ[36]/DDR0_DQ[4]	DDR1_ODT20	AW14 MODT_B1	DDR1_ODT20	AW14 MODT_B1	9
MDB37 AT11	DDR1_DQ[37]/DDR0_DQ[5]	DDR1_ODT21	AW14 MODT_B1	DDR1_ODT21	AW14 MODT_B1	9
MDB38 AP10	DDR1_DQ[38]/DDR0_DQ[6]	DDR1_ODT22	AW14 MODT_B1	DDR1_ODT22	AW14 MODT_B1	9
MDB39 AN10	DDR1_DQ[39]/DDR0_DQ[7]	DDR1_ODT23	AW14 MODT_B1	DDR1_ODT23	AW14 MODT_B1	9
MDB40 AB8	DDR1_DQ[40]/DDR0_DQ[8]	DDR1_ODT24	AW14 MODT_B1	DDR1_ODT24	AW14 MODT_B1	9
MDB41 AT8	DDR1_DQ[41]/DDR0_DQ[9]	DDR1_ODT25	AW14 MODT_B1	DDR1_ODT25	AW14 MODT_B1	9
MDB42 AT5	DDR1_DQ[42]/DDR0_DQ[10]	DDR1_ODT26	AW14 MODT_B1	DDR1_ODT26	AW14 MODT_B1	9
MDB43 AT6	DDR1_DQ[43]/DDR0_DQ[11]	DDR1_ODT27	AW14 MODT_B1	DDR1_ODT27	AW14 MODT_B1	9
MDB44 AP8	DDR1_DQ[44]/DDR0_DQ[12]	DDR1_ODT28	AW14 MODT_B1	DDR1_ODT28	AW14 MODT_B1	9
MDB45 AT7	DDR1_DQ[45]/DDR0_DQ[13]	DDR1_ODT29	AW14 MODT_B1	DDR1_ODT29	AW14 MODT_B1	9
MDB46 AP5	DDR1_DQ[46]/DDR0_DQ[14]	DDR1_ODT30	AW14 MODT_B1	DDR1_ODT30	AW14 MODT_B1	9
MDB47 AR5	DDR1_DQ[47]/DDR0_DQ[15]	DDR1_ODT31	AW14 MODT_B1	DDR1_ODT31	AW14 MODT_B1	9
MDB48 AM8	DDR1_DQ[48]/DDR0_DQ[16]	DDR1_ODT32	AW14 MODT_B1	DDR1_ODT32	AW14 MODT_B1	9
MDB49 AM7	DDR1_DQ[49]/DDR0_DQ[17]	DDR1_ODT33	AW14 MODT_B1	DDR1_ODT33	AW14 MODT_B1	9
MDB50 AK6	DDR1_DQ[50]/DDR0_DQ[18]	DDR1_ODT34	AW14 MODT_B1	DDR1_ODT34	AW14 MODT_B1	9
MDB51 AM5	DDR1_DQ[51]/DDR0_DQ[19]	DDR1_ODT35	AW14 MODT_B1	DDR1_ODT35	AW14 MODT_B1	9
MDB52 AM6	DDR1_DQ[52]/DDR0_DQ[20]	DDR1_ODT36	AW14 MODT_B1	DDR1_ODT36	AW14 MODT_B1	9
MDB53 AK7	DDR1_DQ[53]/DDR0_DQ[21]	DDR1_ODT37	AW14 MODT_B1	DDR1_ODT37	AW14 MODT_B1	9
MDB54 AK5	DDR1_DQ[54]/DDR0_DQ[22]	DDR1_ODT38	AW14 MODT_B1	DDR1_ODT38	AW14 MODT_B1	9
MDB55 AL5	DDR1_DQ[55]/DDR0_DQ[23]	DDR1_ODT39	AW14 MODT_B1	DDR1_ODT39	AW14 MODT_B1	9
MDB56 AF7	DDR1_DQ[56]/DDR0_DQ[24]	DDR1_ODT40	AW14 MODT_B1	DDR1_ODT40	AW14 MODT_B1	9
MDB57 AH9	DDR1_DQ[57]/DDR0_DQ[25]	DDR1_ODT41	AW14 MODT_B1	DDR1_ODT41	AW14 MODT_B1	9
MDB58 AG5	DDR1_DQ[58]/DDR0_DQ[26]	DDR1_ODT42	AW14 MODT_B1	DDR1_ODT42	AW14 MODT_B1	9
MDB59 AF6	DDR1_DQ[59]/DDR0_DQ[27]	DDR1_ODT43	AW14 MODT_B1	DDR1_ODT43	AW14 MODT_B1	9
MDB60 AH6	DDR1_DQ[60]/DDR0_DQ[28]	DDR1_ODT44	AW14 MODT_B1	DDR1_ODT44	AW14 MODT_B1	9
MDB61 AH7	DDR1_DQ[61]/DDR0_DQ[29]	DDR1_ODT45	AW14 MODT_B1	DDR1_ODT45	AW14 MODT_B1	9
MDB62 AF5	DDR1_DQ[62]/DDR0_DQ[30]	DDR1_ODT46	AW14 MODT_B1	DDR1_ODT46	AW14 MODT_B1	9
MDB63 AH5	DDR1_DQ[63]/DDR0_DQ[31]	DDR1_ODT47	AW14 MODT_B1	DDR1_ODT47	AW14 MODT_B1	9

2 OF 13

CPU-SK/1200/S/GF

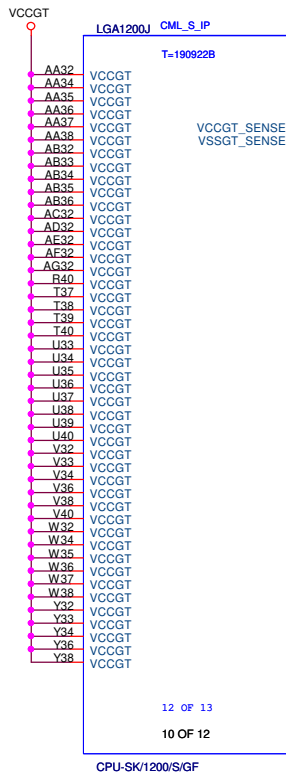
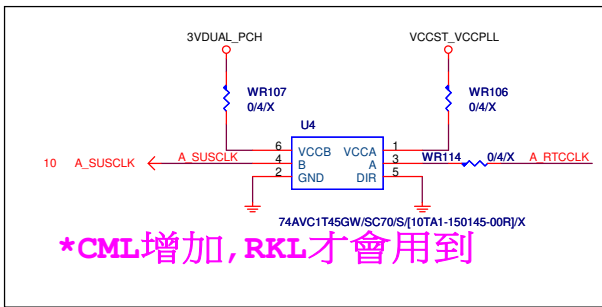
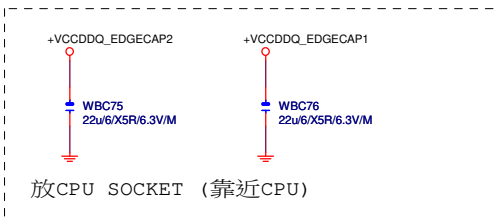
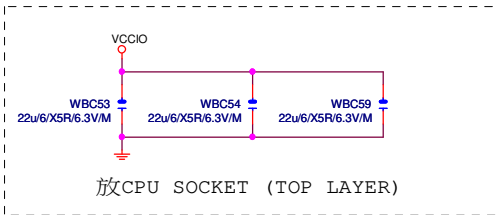
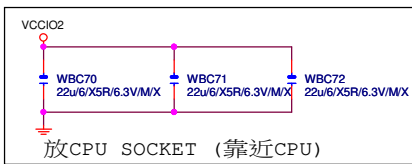
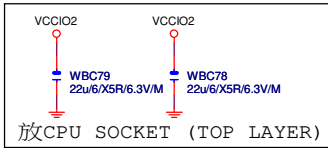
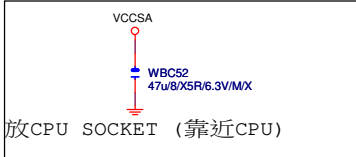
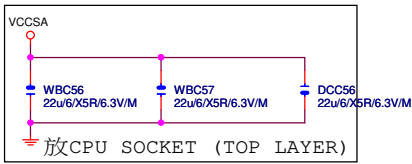


黑色cover

LGA1200  
ILM\_BP\_CR/115X/BKNI/12KRC-SF0001-83R\_12KRC-SF0001-84R

8	MDA[0..63]	MDA[0..63]
9	MDB[0..63]	MDB[0..63]
8	M_DQSA[0..7]	M_DQSA[0..7]
8	M_-DQSA[0..7]	M_-DQSA[0..7]
8	MAAA[0..16]	MAAA[0..16]
9	MAAB[0..16]	MAAB[0..16]
9	M_DQSB[0..7]	M_DQSB[0..7]
9	M_-DQSB[0..7]	M_-DQSB[0..7]

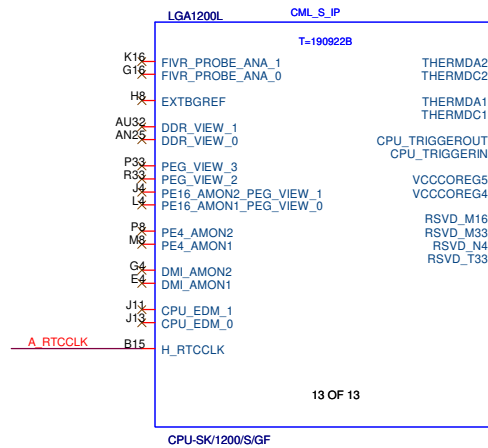
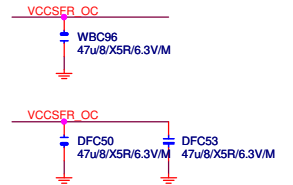
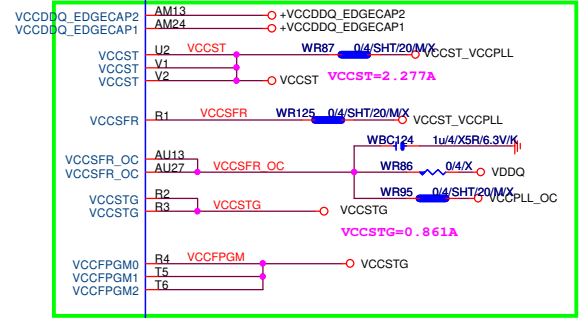
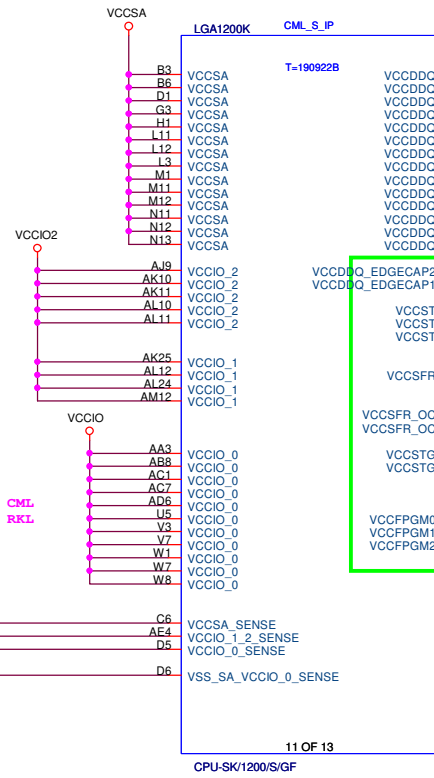
Gigabyte Technology		
CPU LGA1200-B		
Title	Document Number	Rev
Size	H510M H	1.0
Custom		
Date:	Wednesday, January 06, 2021	Sheet 5 of 62



VCCIO\_1\_2  
VOUT = 0.95V  
IOUT = 9.5A

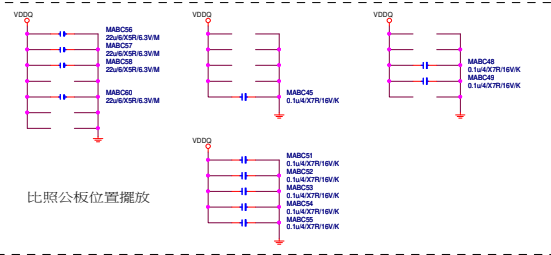
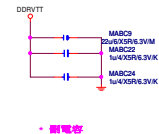
VCCIO\_0  
VOUT = 0.95V FOR CML  
VOUT = 1.05V FOR RKL  
IOUT = 8A

59 VCCSA\_SENSE  
58 VCCIO2\_SENSE  
57 VCCIO\_SENSE  
57,59 VSSSA\_VIO\_SENSE

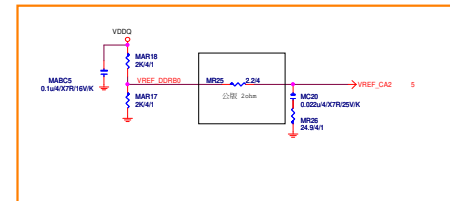
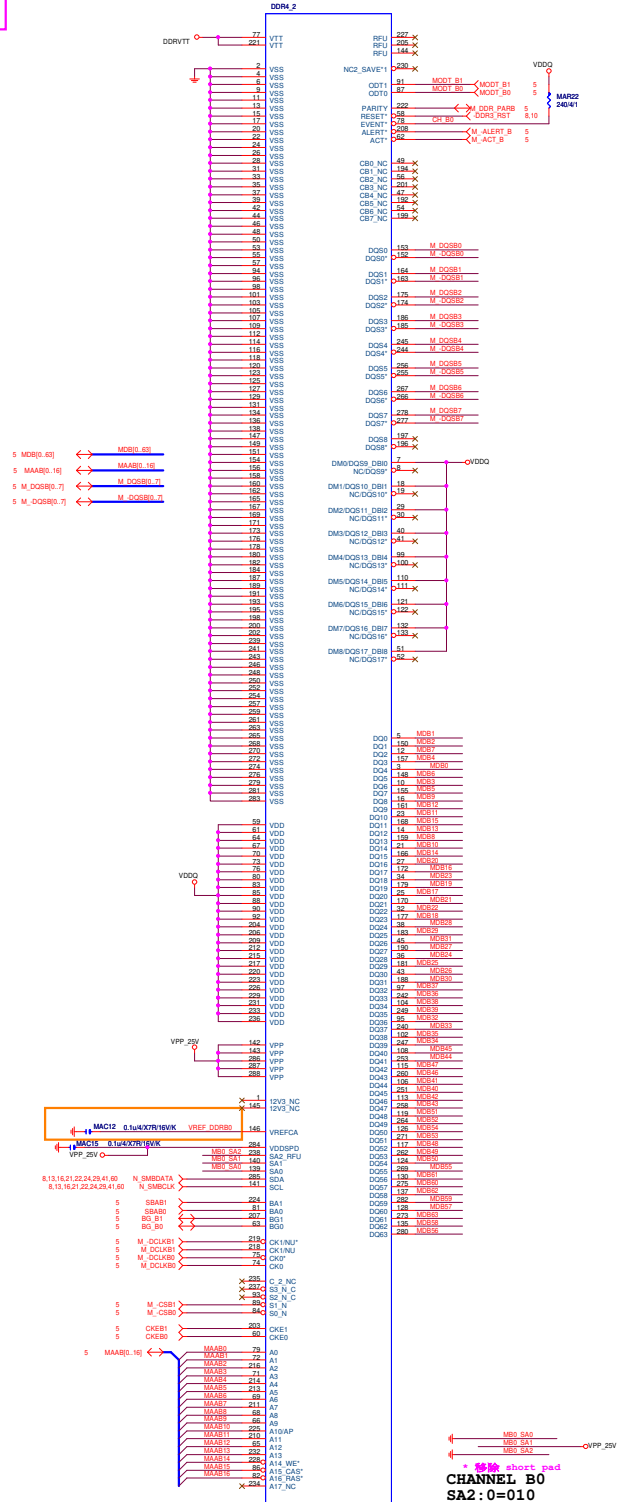


10 N\_CPUPTCLK → WR113 0/4 A\_RTCCLK



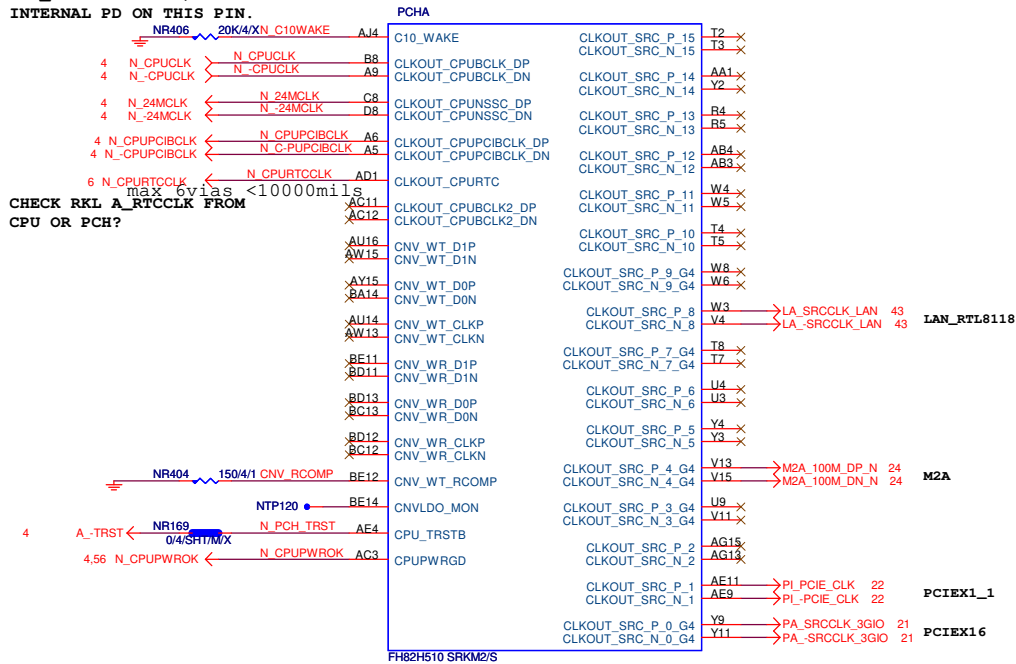




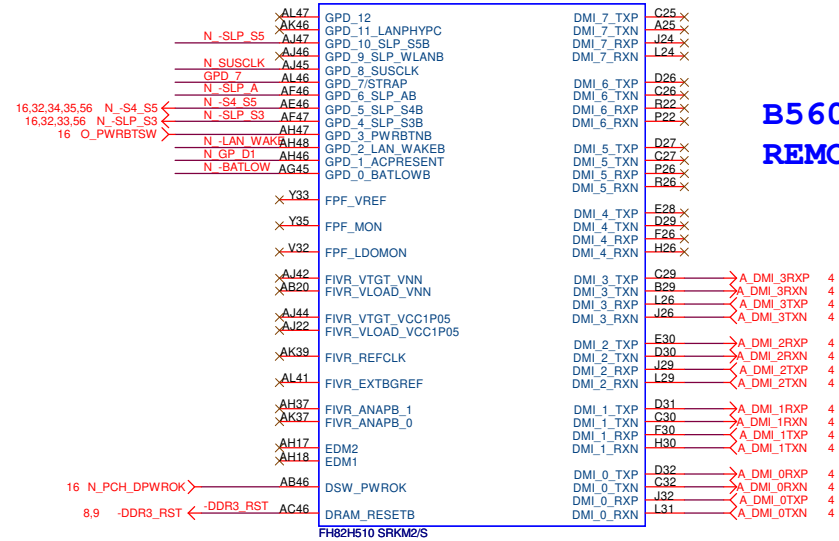


# RKL\_TGP\_PCH-H R0.11

C10\_WAKE RESERVED/BIOS NEED TO PROGRAM  
INTERNAL PD ON THIS PIN.



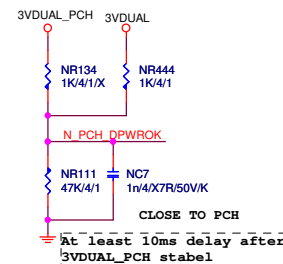
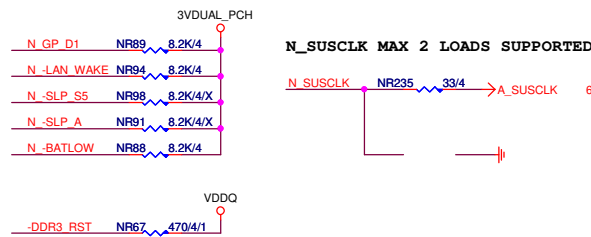
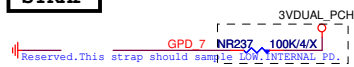
## PCHB



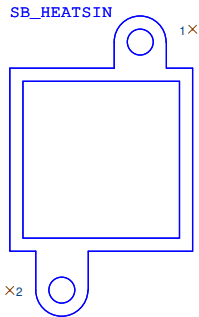
B560/H510  
REMOVE DMI4~7

CLKOUT\_PCIE\_P/N [9, 7, 4, 3, 0] = Must be used for PCIe\* Gen4 support

## STRAP



PCH Signal Glitch Free

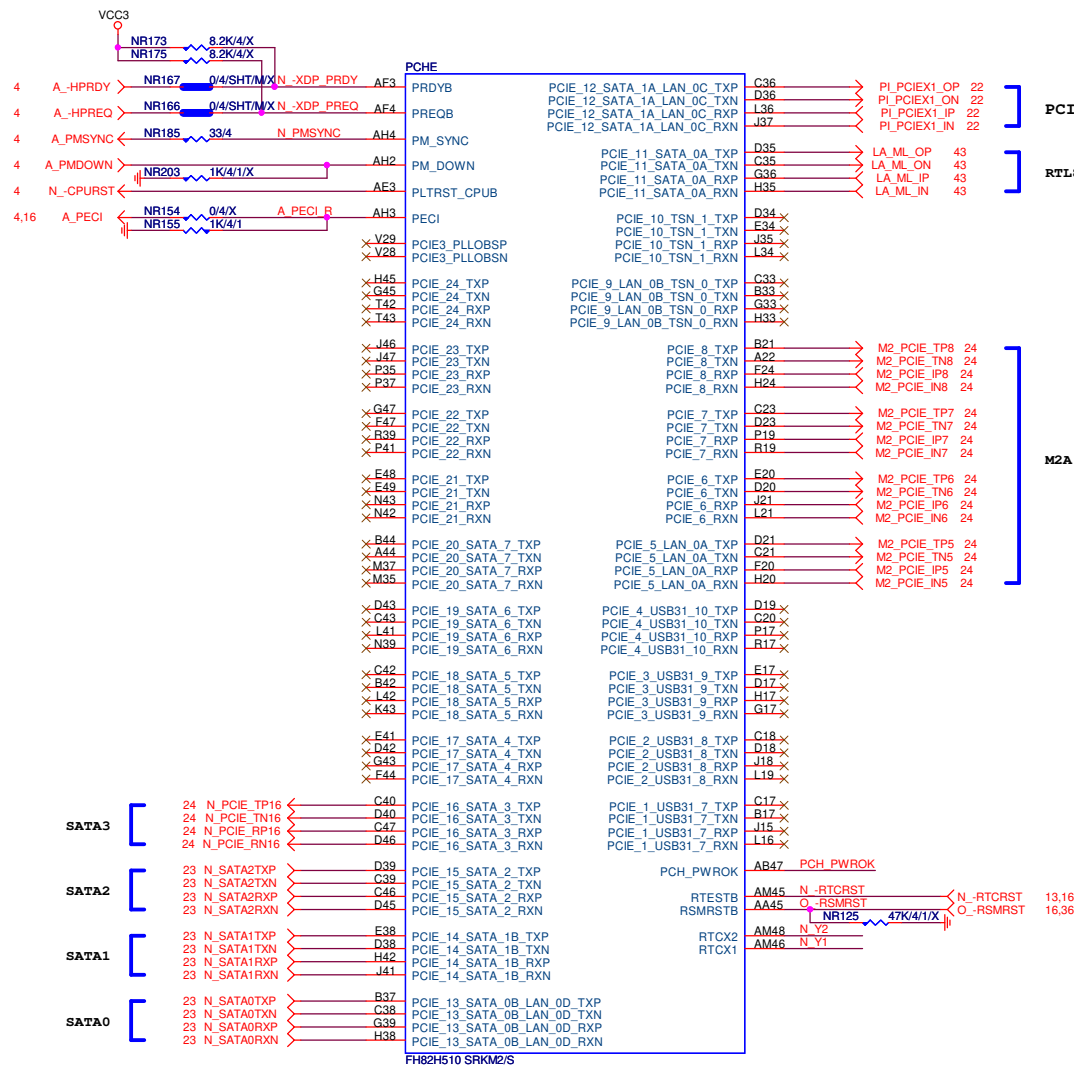


業務指定使用B150M-EVO Heatsink

ANS 8477624		Gigabyte Technology	
Title		PCH CLOCK BUFFER	
Size	Document Number	Rev	
Custom	H510M H	1.0	
Date:	Wednesday, January 06, 2021	Sheet	10 of 62

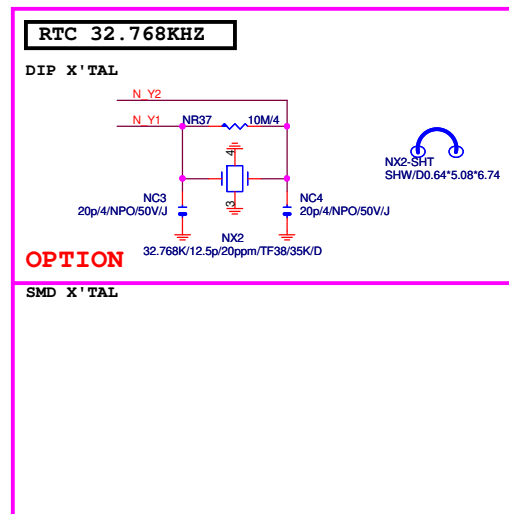


# RKL\_TGP\_PCH-H R0.11



Intel 500 series PCH PCIE P5~P12								
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11	PCIE P12
H510	PCIE /GbE	PCIE	PCIE	PCIE	GbE ONLY	N/A	PCIE	PCIE /GbE
B560	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
H570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Z590	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Q570	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
W580	PCIE /GbE	PCIE	PCIE	PCIE	PCIE /GbE	PCIE	PCIE SATA_0'	PCIE SATA_1' GbE
Intel® RST for x2/x4 M.2								

Intel 500 series PCH PCIE P13~P24												
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23	PCIE P24
H510	SATA_0 /GbE	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 /GbE	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE	PCIE
H570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 GbE	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE	PCIE
Intel® RST for x2/x4 M.2									Intel® RST for x2/x4 M.2			



Intel 500 series PCH USB P7~P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
	PCIE	PCIE	PCIE	PCIE
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	PCIE	PCIE	PCIE	PCIE





NRN9 33/8P4R/4

Signal	Pin	Signal
45 C_ACZ_BITCLK	1	HDA BCLK
45 C_ACZ_SYNC	3	HDA SYNC
45 C_ACZ_SDOUT	5	HDA SDO
45 C_ACZ_RST	7	HDA RST

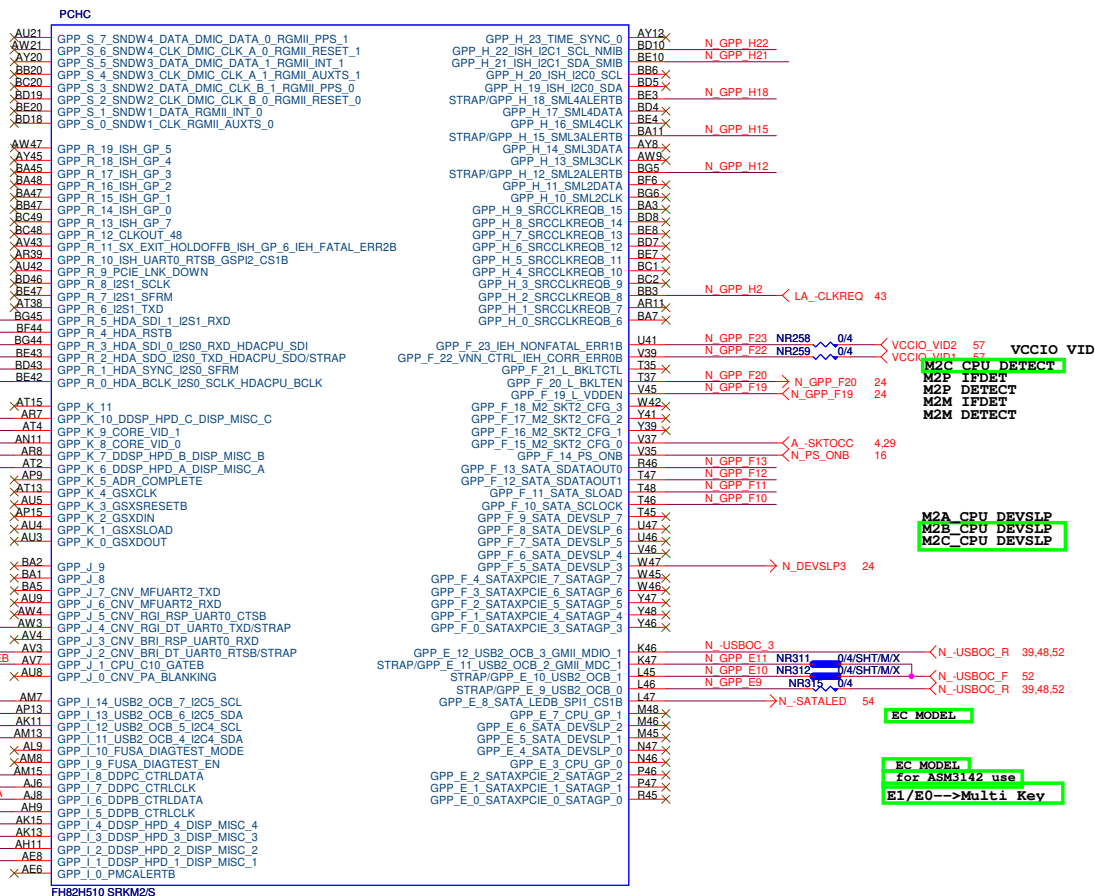
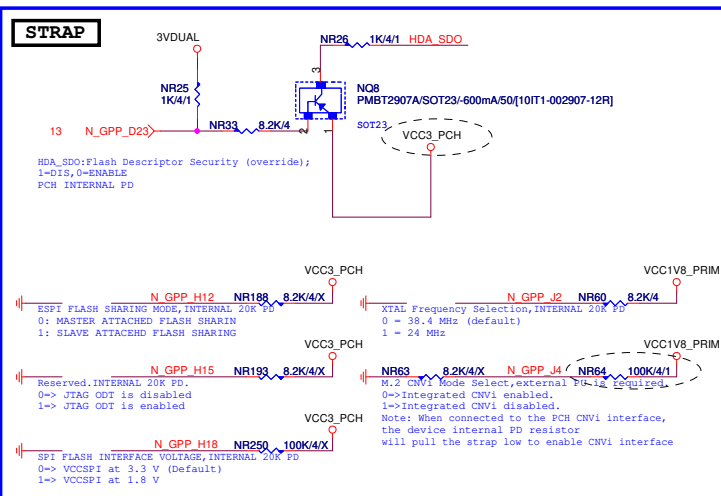


```
TBT RTD3
M2B CPU DETECT
M2A CPU IFDET
M2A CPU DETECT
```

J GROUP ONLY 1.8V LEVEL

\*\*DDPC CHANGE TO GPP\_G12/G13

U32GEN2\*2 C.C DETECT



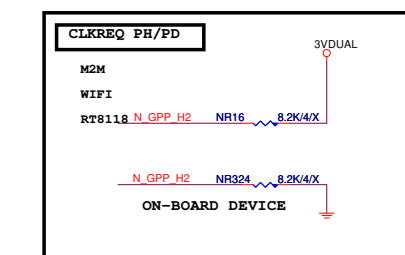
Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP\_J and GPP\_S (1.8 V/VCCPRIM\_1P8)

Display Port DDC/HOT PLUG SIGNAL		
CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2

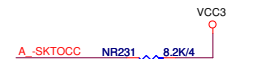
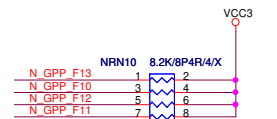
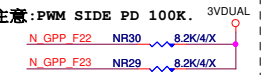
\*\*\*  
HPD: DDI\*. PULL DOWN IF NO USE.

A	N_GPP_K6	NR233	100K/4/I	
B	N_GPP_K7	NR236	100K/4/X	DP to VGA
C	N_GPP_K10	NR273	100K/4/I	
D	N_GPP_I1	NR238	100K/4/I	
E	N_GPP_I2	NR270	100K/4/X	
F	N_GPP_I3	NR272	100K/4/I	
G	N_GPP_I4	NR271	100K/4/I	

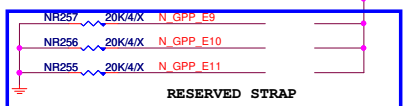
PCH Signal Glitch Free



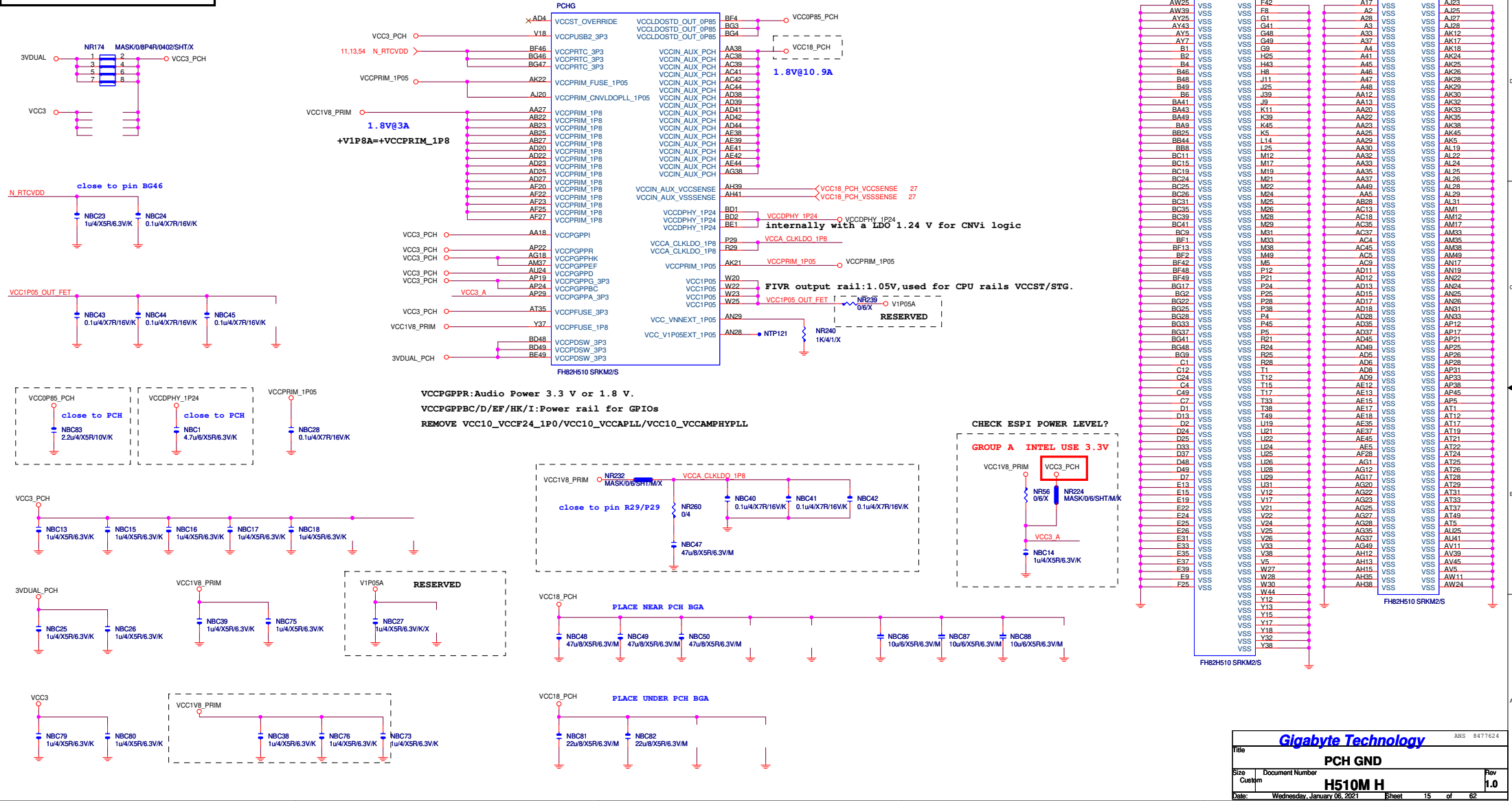
注意: PWM SIDE PD 100K.



Internal pull up



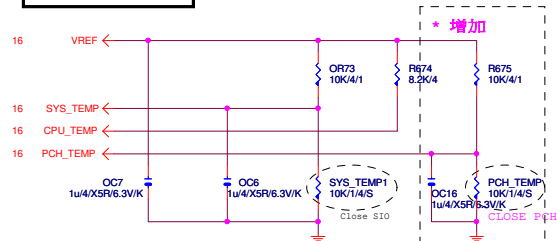
RTD3 GPIO	CML-S	RKL-S
TBT_PERST_N <sup>o</sup>	GPP_F2 <sup>o</sup>	GPP_F16 <sup>o</sup>
TBT_Wake_N <sup>o</sup>	GPP_H15 <sup>o</sup>	GPP_H9 <sup>o</sup>
RTD3_PWN_EN	GPP_K23 <sup>o</sup>	GPP_K3 <sup>o</sup>



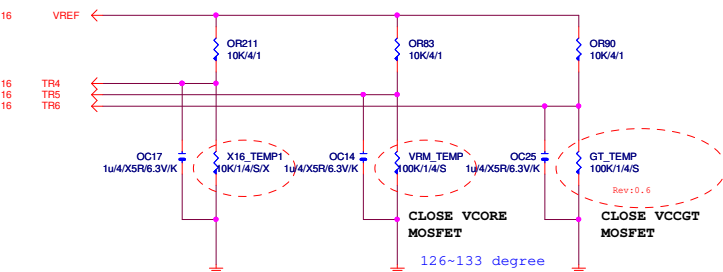




## TEMP H/W MONITOR

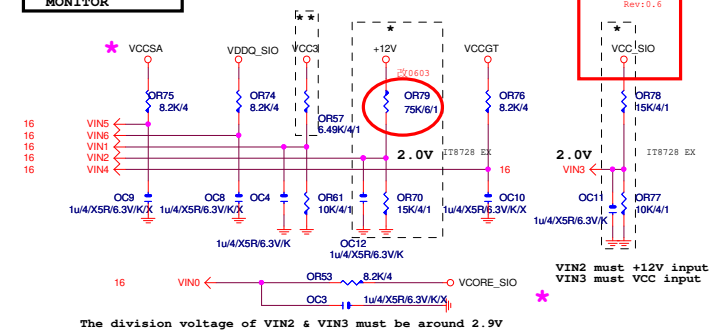


**低階機種:3個FAN時使用**

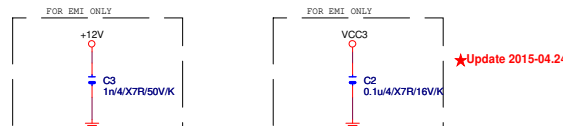


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VOLTAGE-- H/W  
MONITOR



(靠近ATX CONNECTOR )

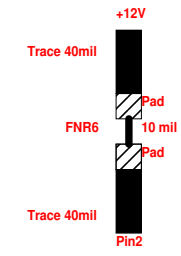
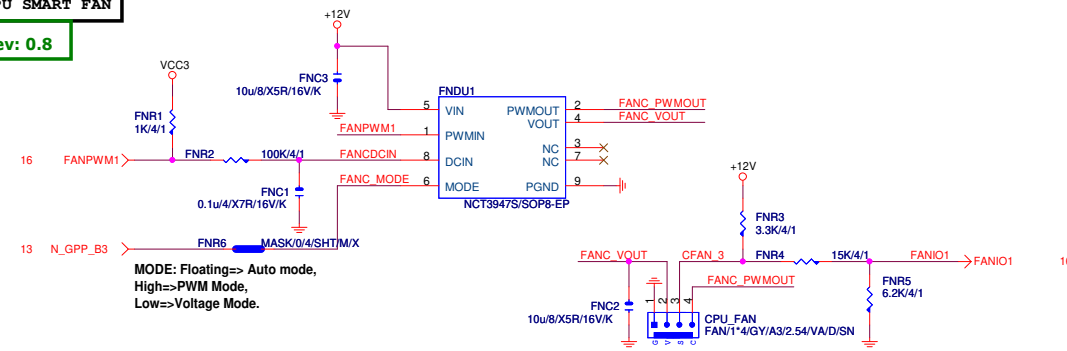


## Gigabyte Technology

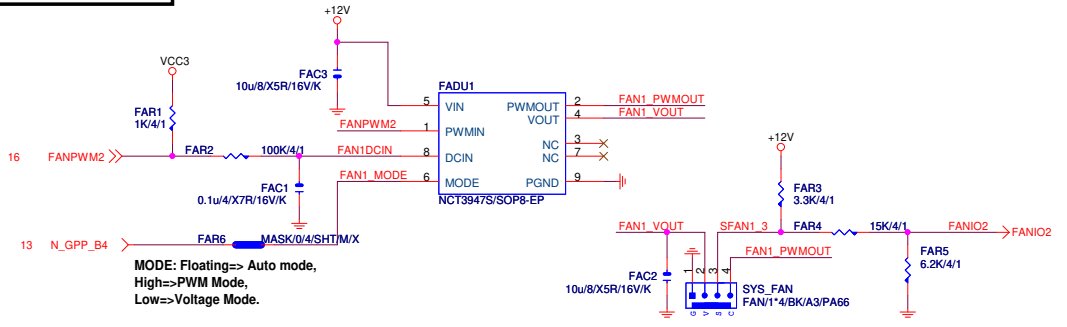
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HWM,KB/MS, FAN CTRL			
Size	Document Number		Rev
Custom	H510M H		1.0
Date:	Wednesday, January 06, 2021	Sheet	17 of 62

CPU SMART FAN

Rev: 0.8



A. SYSTEM FAN1

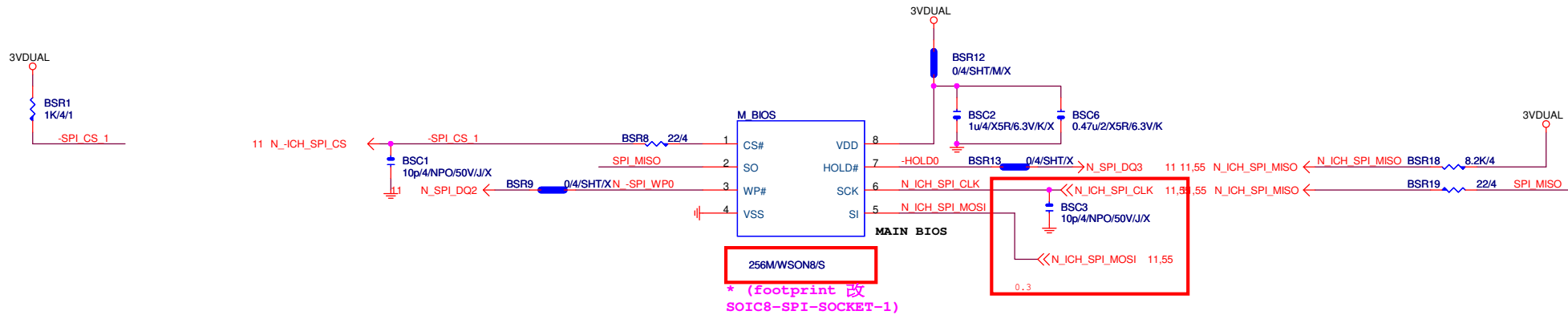


Gigabyte Technology

Title			
FAN CTRL			
Size	Document Number	Rev	
Custom	H510M H	1.0	
Date:	Wednesday, January 06, 2021	Sheet	18 of 62

DUAL BIOS

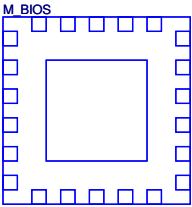
MOSI For DMI RX Termination Voltage



256M/WSN8/S  
\* (footprint 改  
SOIC8-SPI-SOCKET-1)

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating  
0 means PD 1K




SMD WSON8 SK 8P 200MIL LOTES[10SL2-000008-71R]/X

\* 試産先上, PVT 移除

Gigabyte Technology

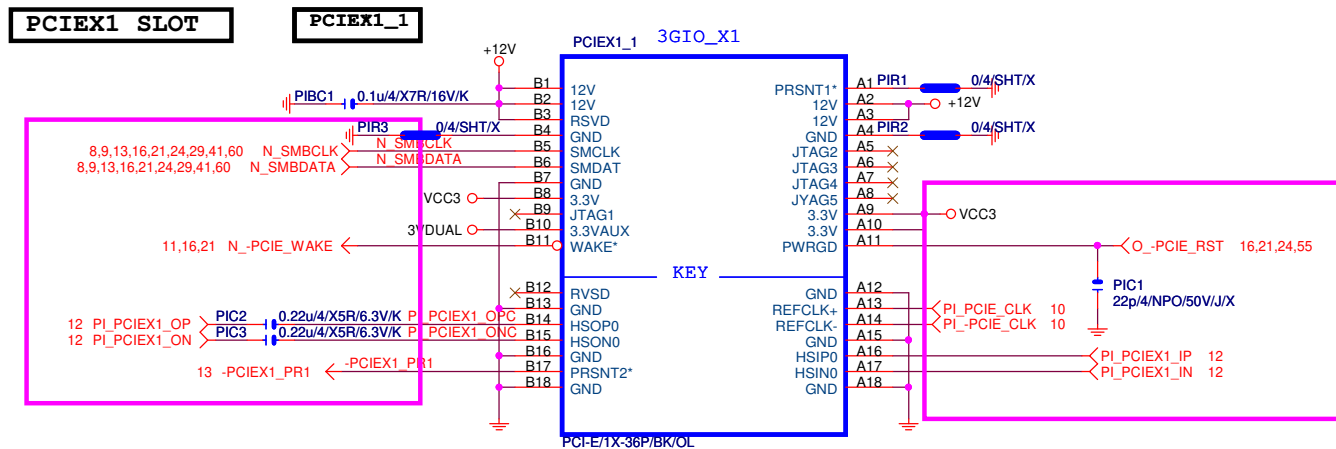
Title			BIOS
Size	Document Number	H510M H	
Custom		Rev	1.0
Date:	Wednesday, January 06, 2021	Sheet	19 of 62

CEC\_R0.3

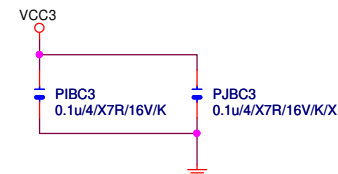


Title			
CEC relate circuit			
Size	Document Number	Rev	
Custom	H510M H	1.0	
Date:	Wednesday, January 06, 2021	Sheet	20 of 62





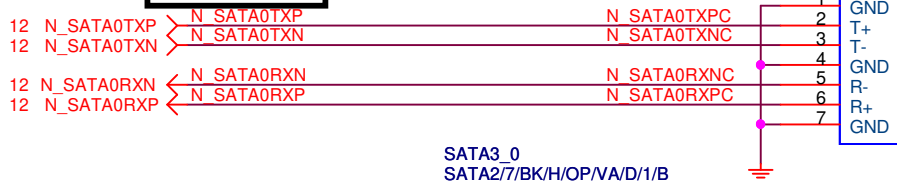
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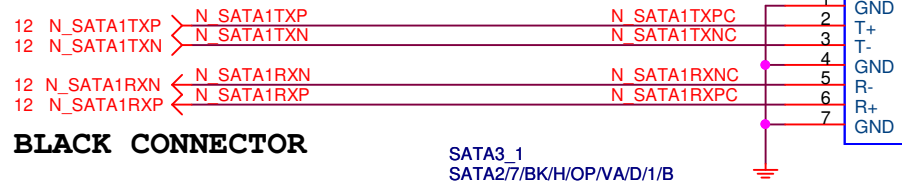
Gigabyte Technology

Title		
PCIE X4		
Size	Document Number	Rev
Custom	H510M H	1.0
Date:	Wednesday, January 06, 2021	Sheet 22 of 62

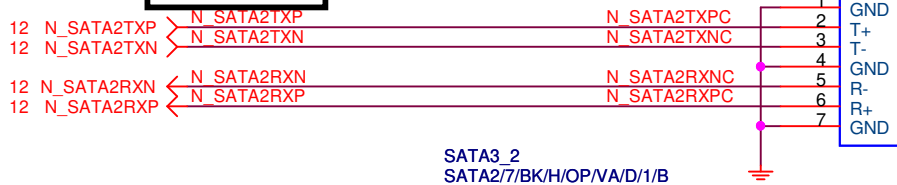
**SATA3 0/1**



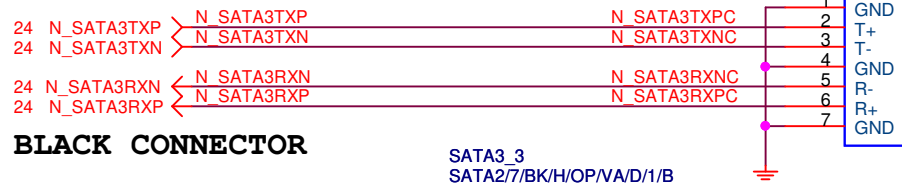
**BLACK CONNECTOR**



**SATA3 2/3**



**BLACK CONNECTOR**



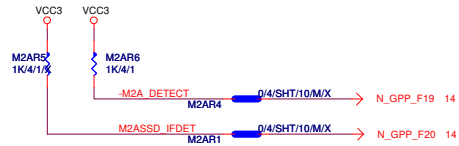
**SATA3 4/5**

**Gigabyte Technology**

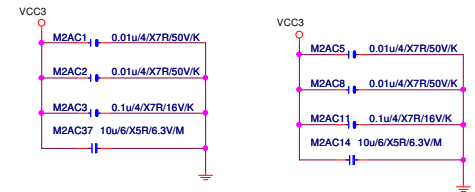
Title		
SATA		
Size	Document Number	Rev
Custom	H510M H	1.0
Date:	Wednesday, January 06, 2021	Sheet 23 of 62



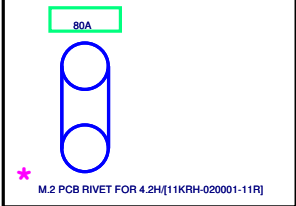
## 支援SATA and M.2 function



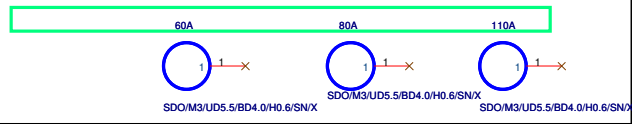
Footprint : NGFF-M-75P-11CM-3-SMD



### M.2 塑膠扣具

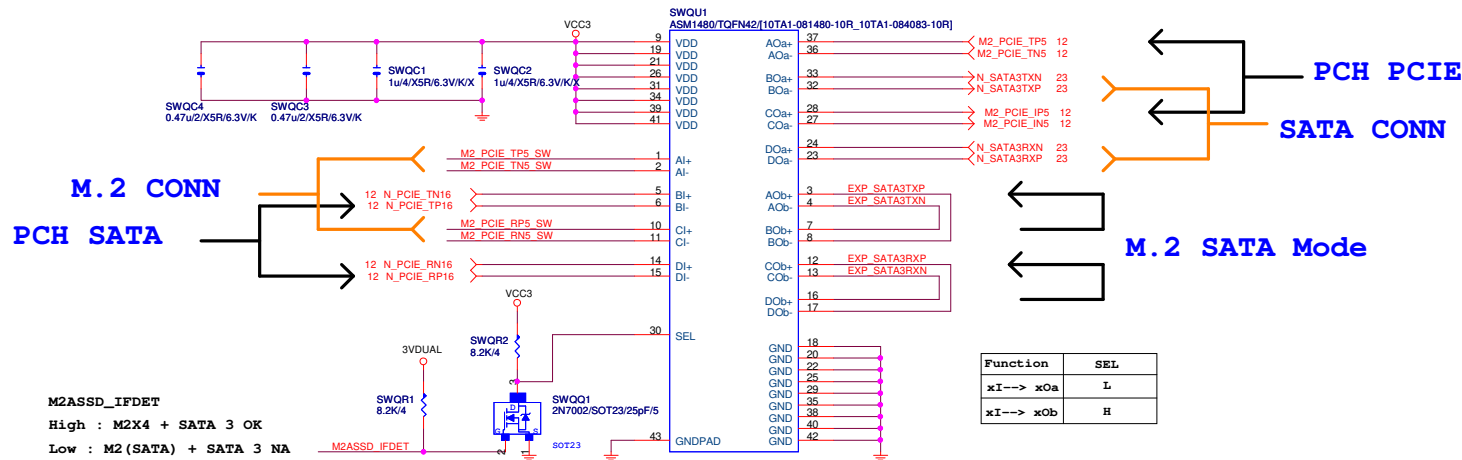


## SMD螺柱



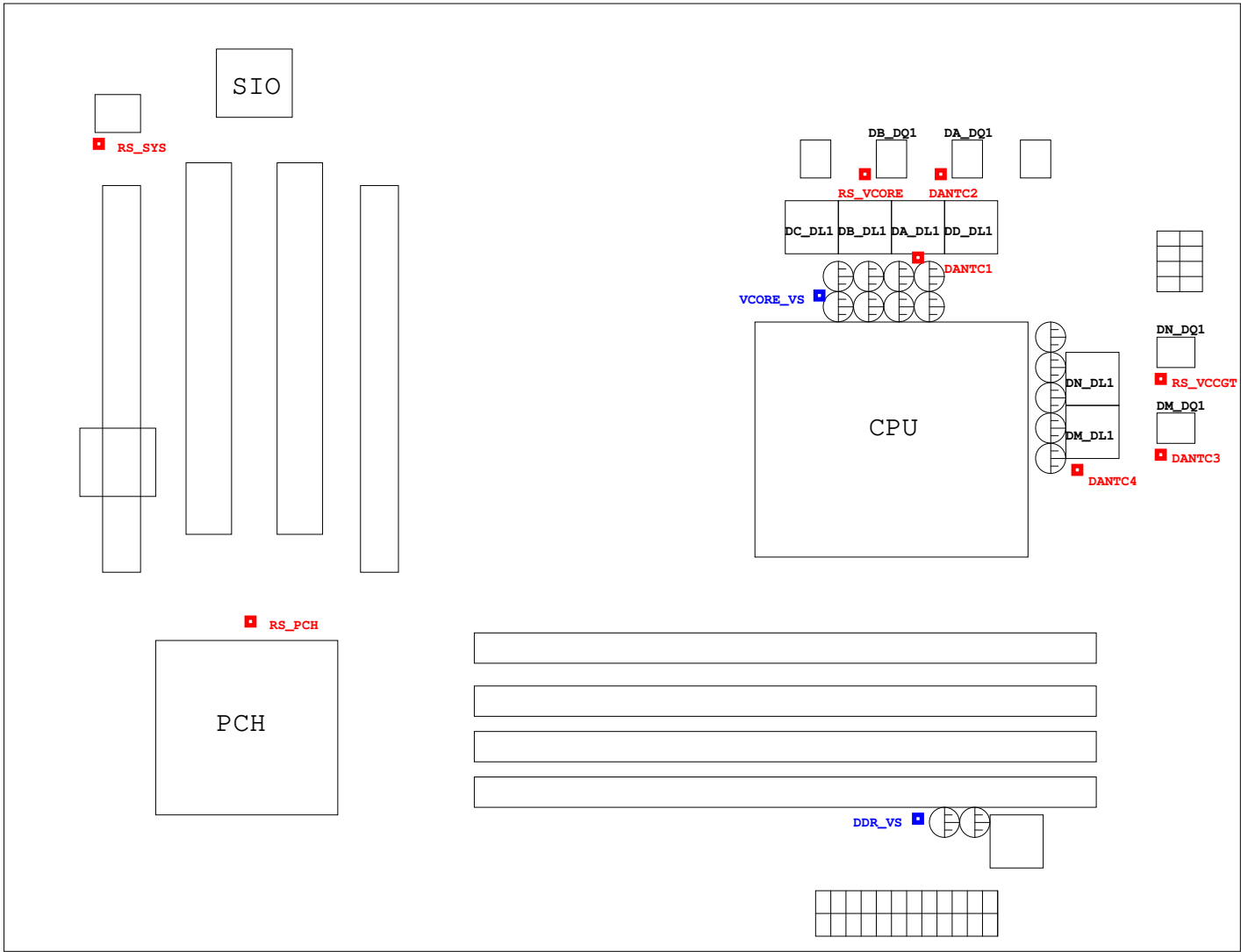
\* Footprint : HOLE\_165NP

舊的Switch,價格低



Function	SEL
<b>xI--&gt; xOa</b>	<b>L</b>
<b>xI--&gt; xOb</b>	<b>H</b>





熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL1	N/A
DANTC2	DA_DQ1	Differential
DANTC3	DM_DQ1	N/A
DANTC4	DM_DL1	Differential
RS_VCORE	DB_DQ1	N/A
RS_VCCGT	DN_DQ1	N/A
RS_PCH	PCH	N/A
RS_SYS	CU1	N/A

5	4	3	2	1
D				D
C				C
B				B
A				A
<div><div><div><div><div>File</div><div>IT8892E</div><div>Size Custom</div><div>Document Number H510M H</div><div>Date: Wednesday, January 06, 2021</div></div><div><div>Rev</div><div>1.0</div><div>Sheet 26 of 62</div></div></div></div></div>				

請自行確認電容要用SMD或DIP

\*改台系固態電容

注意耐壓

100uOS/D/16V/69/A/35m

DCR=7.4 mohm

Isat=15A

Idc=12A

VOUT = 1.8V

ICCMAX = 11.2A

請自行確認電容要用SMD或DIP

\*Del C16,C17,C18

\*改台系固態電容

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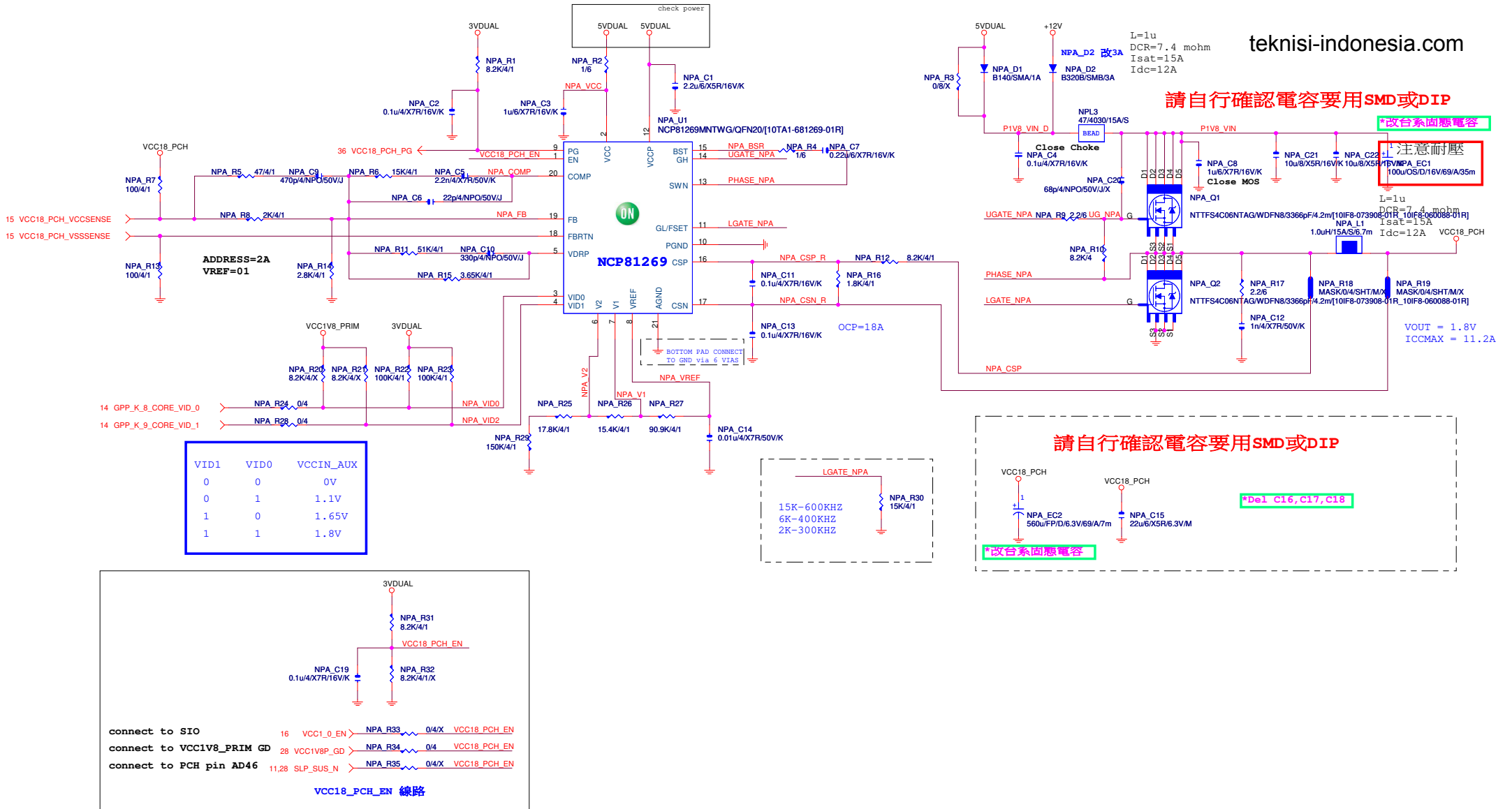
Title NCP81269\_PCH POWER

Size Document Number H510M H

Date: Wednesday, January 06, 2021

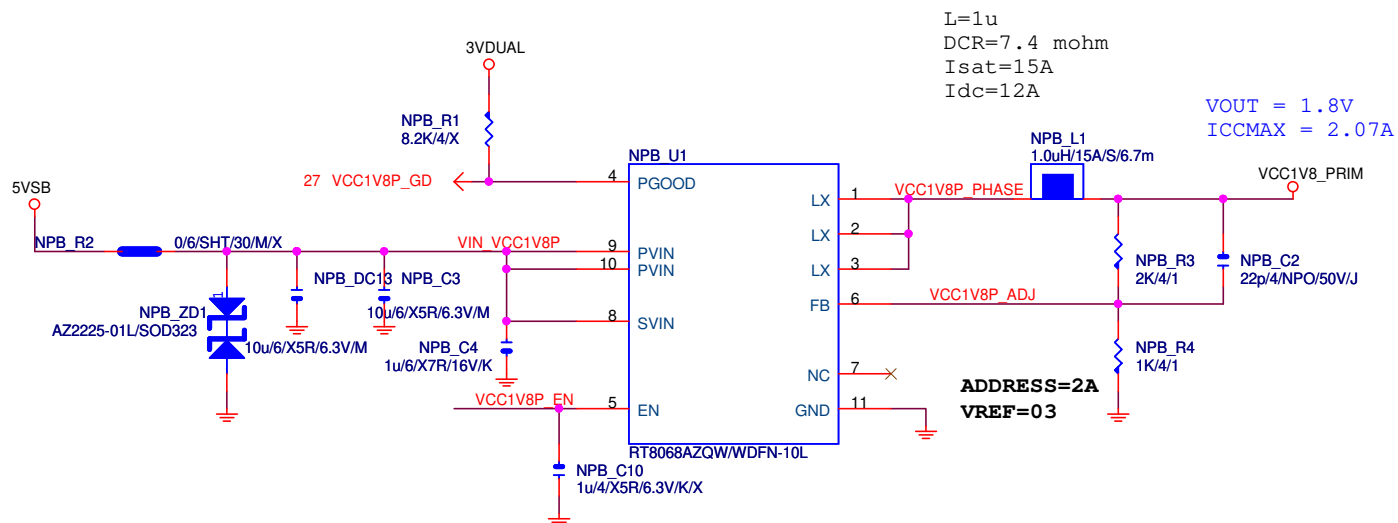
Sheet 27 of 62

Rev 1.0

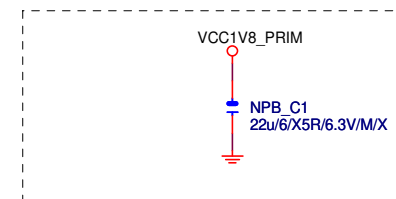


REV:0.1

# VCC1V8 PRIM

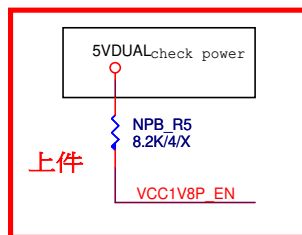


CHOKE與CAP料號可變



請放置CHOKE一出來位置.先預留.  
請自行確認ripple後再決定是否上件

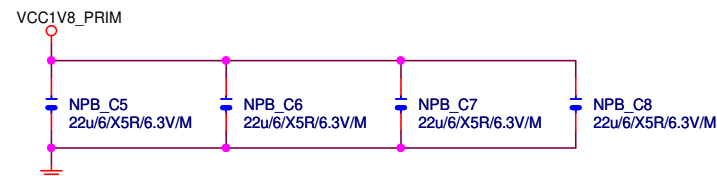
## PWR SEQ



connect to PCH pin AD46

11,27 SLP\_SUS\_N >> NPB\_R6 0/4 VCC1V8P\_EN

## VCC1V8\_PRIM CAP 22u\*4PCS



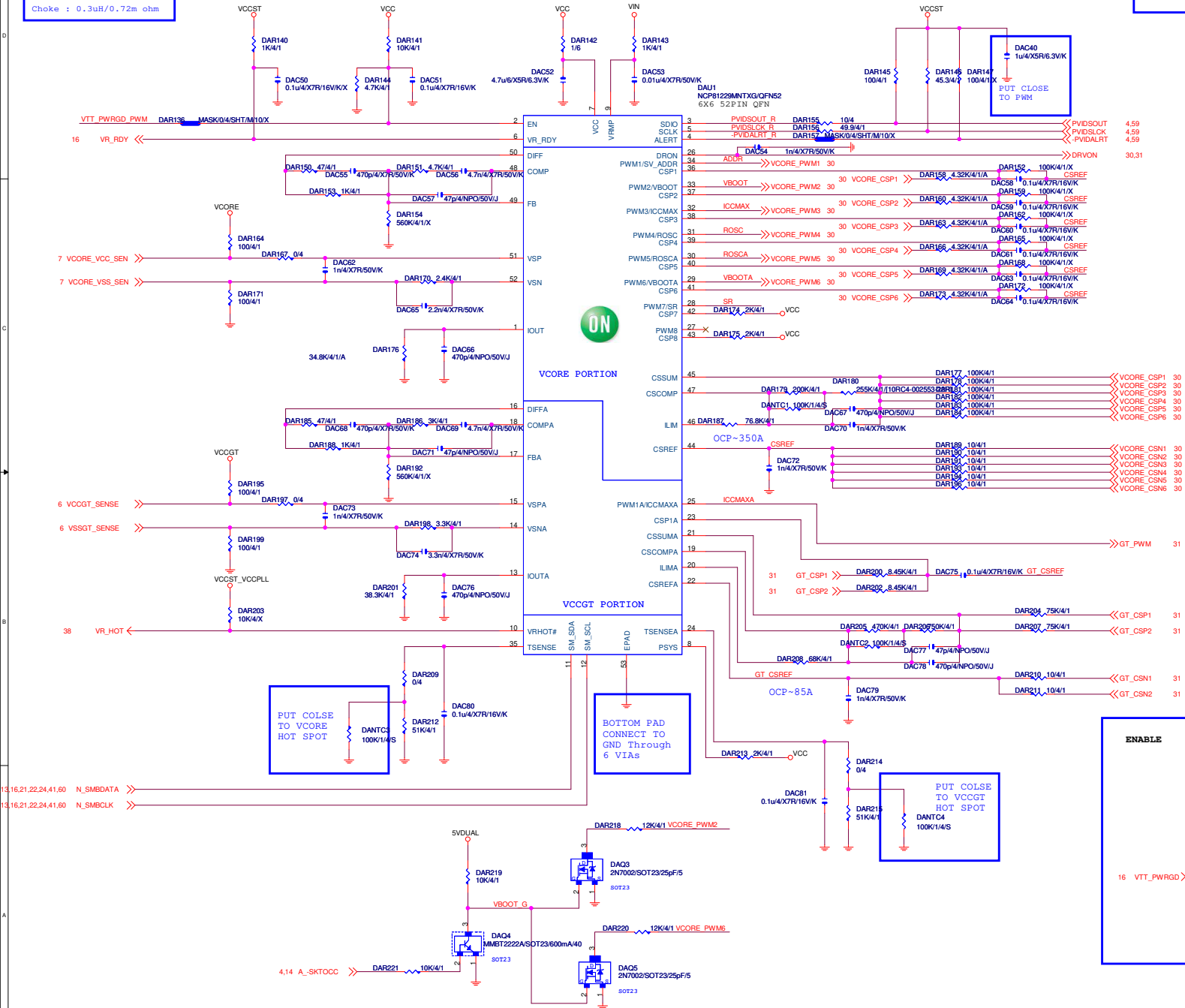
Gigabyte Technology

Title		
RT8068_VCC1V8_PRIM		
Size	Document Number	Rev
Custom	H510M H	1.0
Date:	Wednesday, January 06, 2021	Sheet 28 of 62

Choke : 0.3uH/0.72m ohm

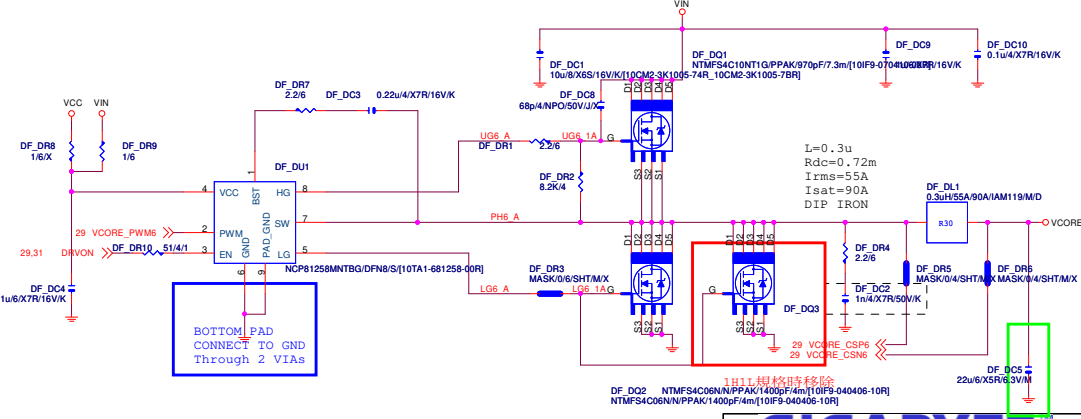
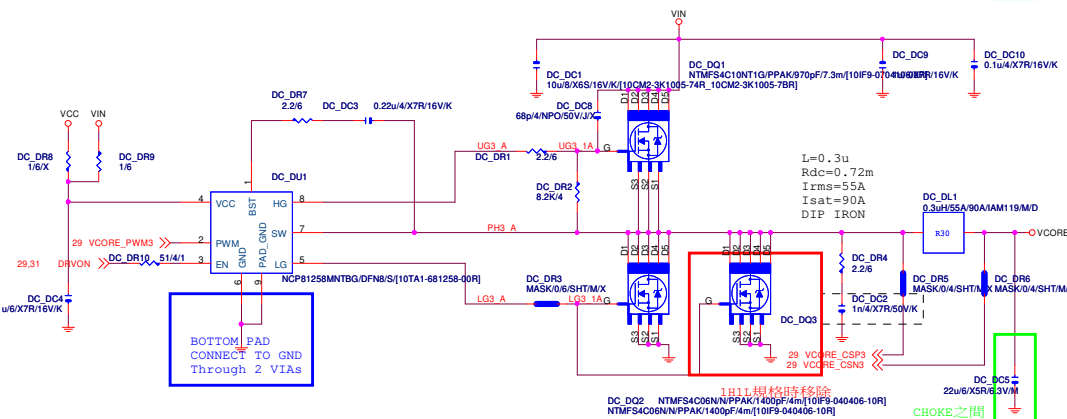
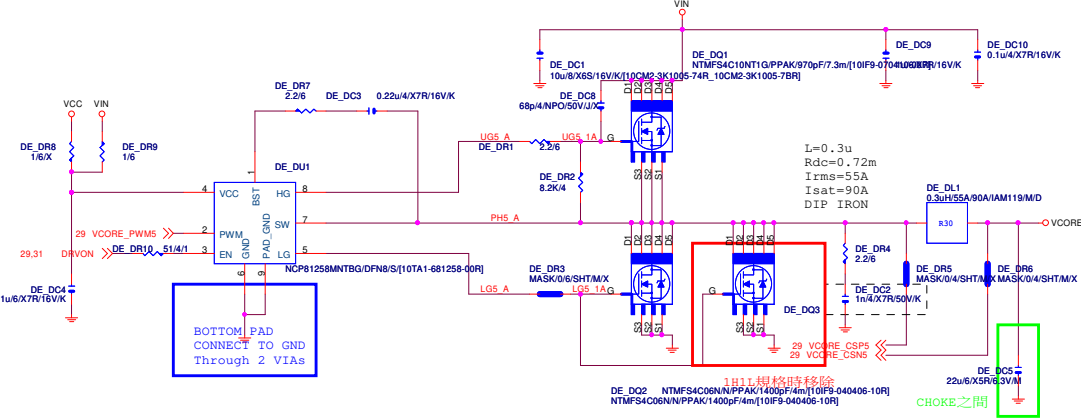
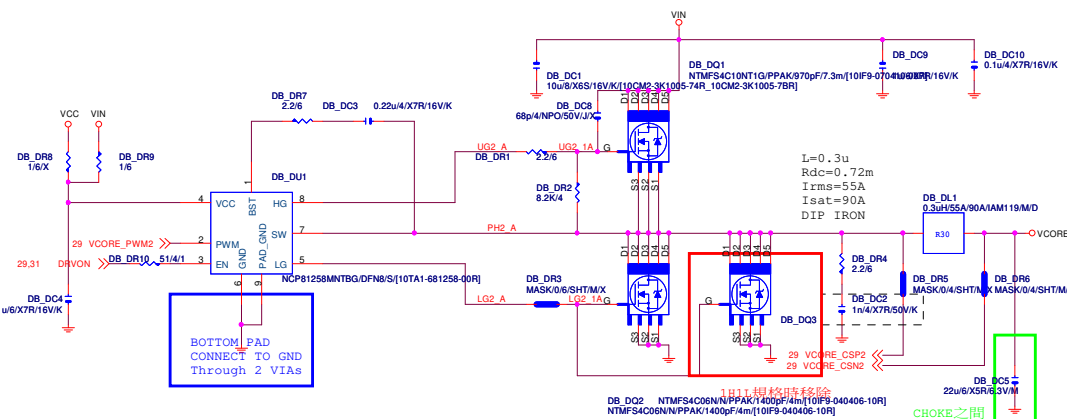
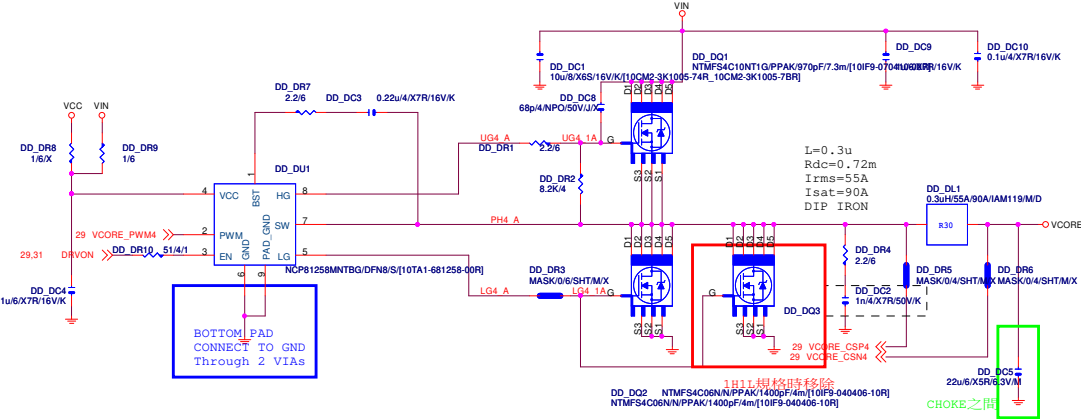
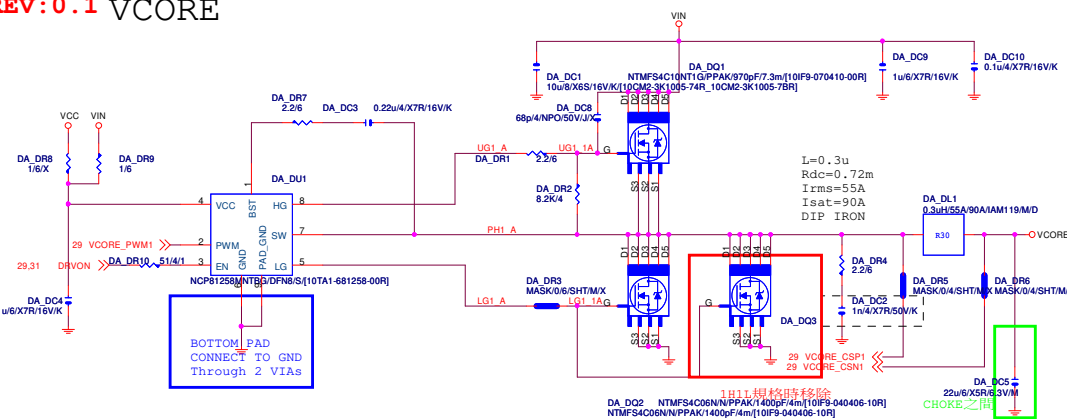
The diagram shows a 4x3 grid of circuit connections. Each cell contains a signal name, its value or setting, and the pin number and package type. The signals are connected to ground via a red line.

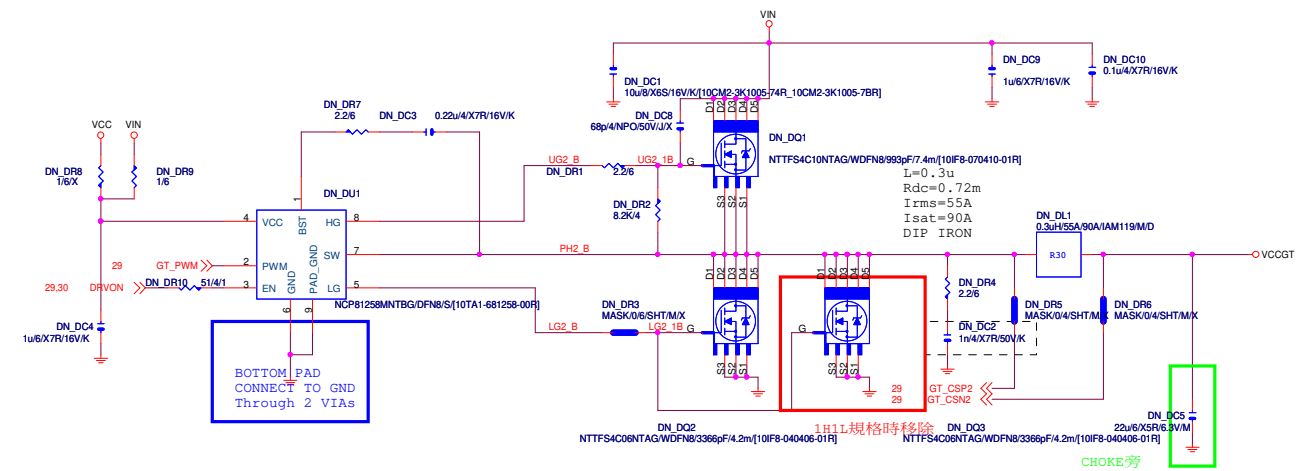
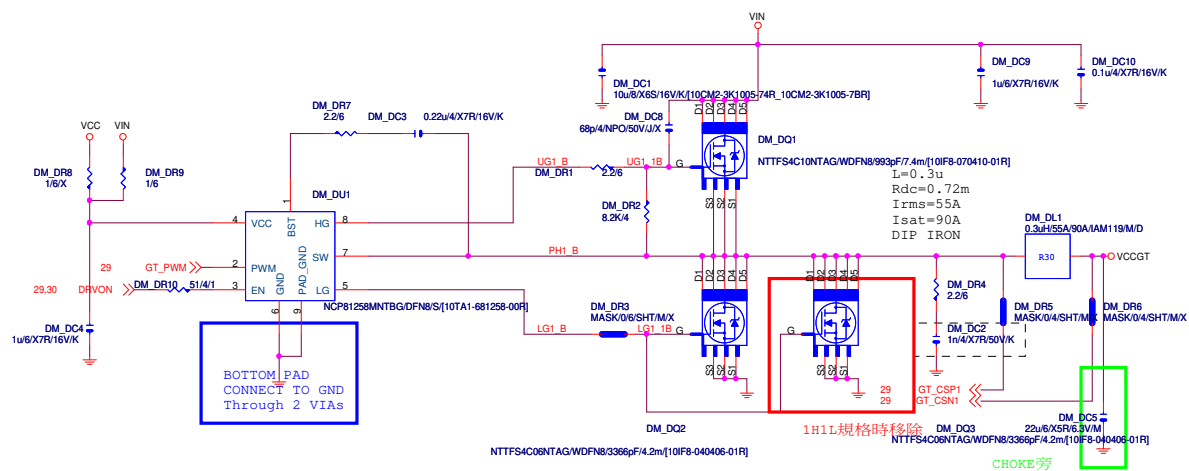
Signal	Value/Setting	Pin	Package
SR	Slew Rate set at 10mV/uS	DAR137	10K/4/1
ADDR	VCORE SVID ADDRESS=00h VCCGT SVID ADDRESS=01h	DAR138	10K/4/1
ICCMAX	VCORE IMAX SET AT 245A	DAR139	243K/4/1
VBOOT	VCORE VBOOT=0V	DAR148	59K/4/1
ICCMAXA	VCCGT IMAX SET AT 55A 54.9K/4/1A	DAR149	
VBOOTA	VCCGT VBOOT=0V	DAR161	59K/4/1
ROSC	VCORE WORKING FREQ ~ 270KHZ	DAR216	21K/4/1
ROSCA	VccGT WORKING FREQ ~ 270KHZ	DAR217	21K/4/1



**Gigabyte Technology**

Title			
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## DDR4



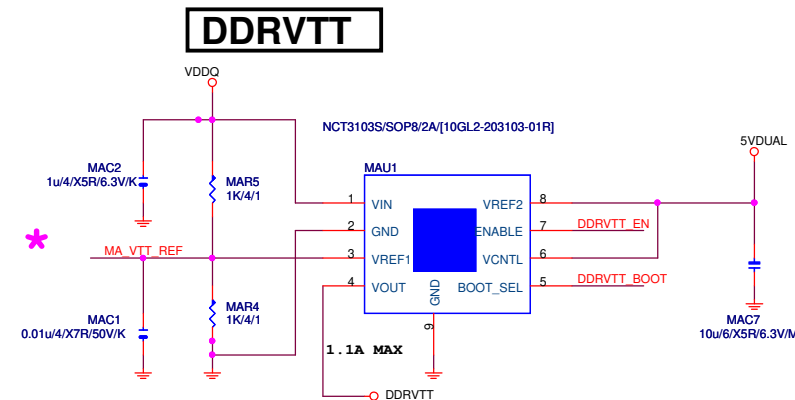
Remote sense 請從最重的負載端點拉回

CLOSE TO DDR POWER PLANE

For power sequence require

VPP\_25V使用8120時上件

MAU1上RT9045時上件(不可MASK)

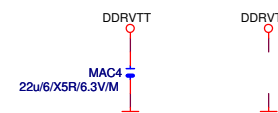


DDR CAP    560u\*4PCS    22u\*2PCS



DDRVTT CAP

\* 大電容 x0



# GIGABYTE

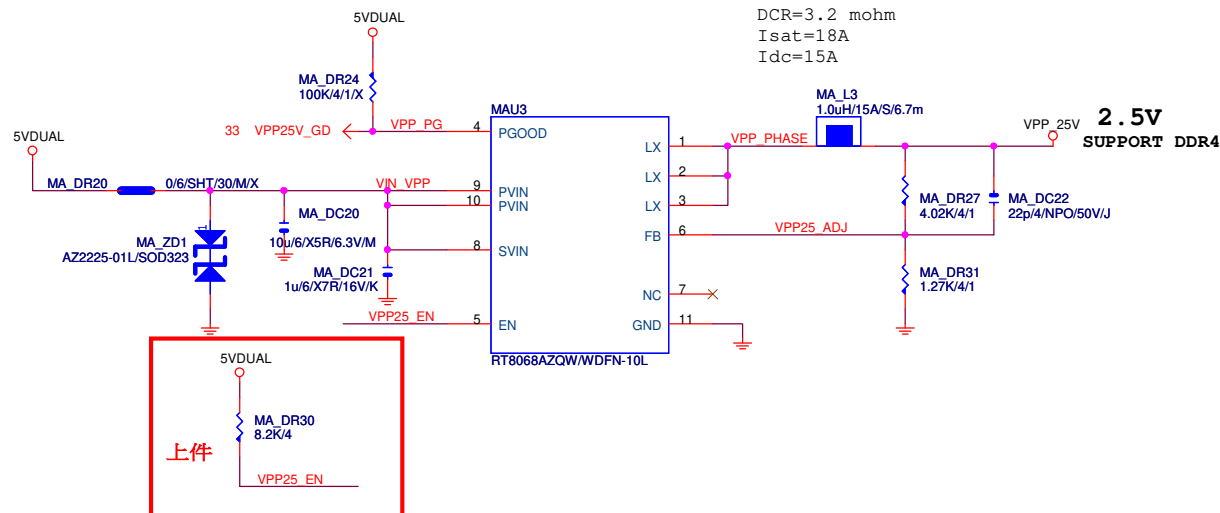
Title			
<b>RT8237_DDR4 POWER</b>			
Size	Document Number		Rev
Custom	<b>H510M H</b>		<b>1.0</b>
Date:	Wednesday, January 06, 2021	Sheet	33 of 62

REV:0.1

VPP 25V

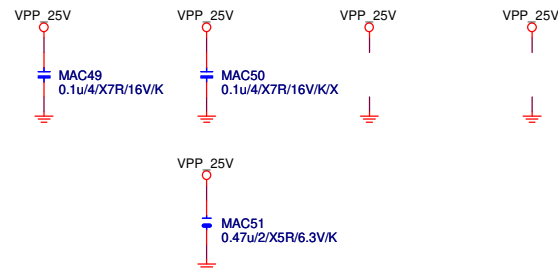
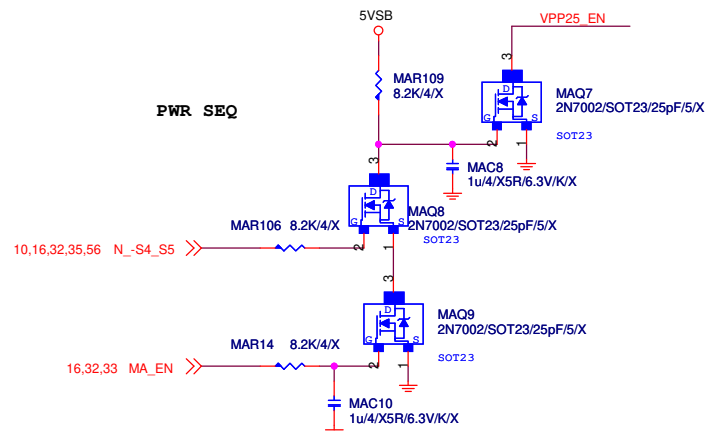
CHOKE與CAP料號可變

L=1u  
DCR=3.2 mohm  
Isat=18A  
Idc=15A



PWR SEQ

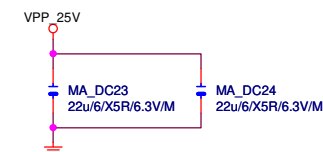
\* 刪 MA\_DR32



16 VPP25\_EN\_IO >> MASK/0/4/SHT/M/X  
MAR114 >> VPP25\_EN

VPP CAP 22u\*1PCS

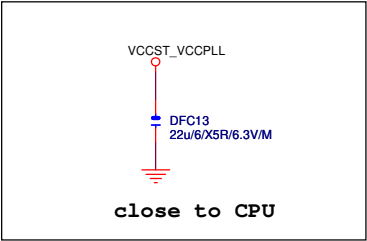
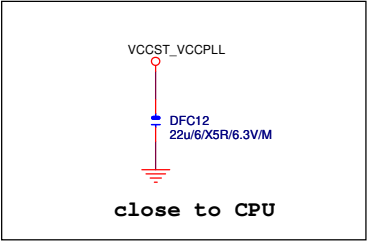
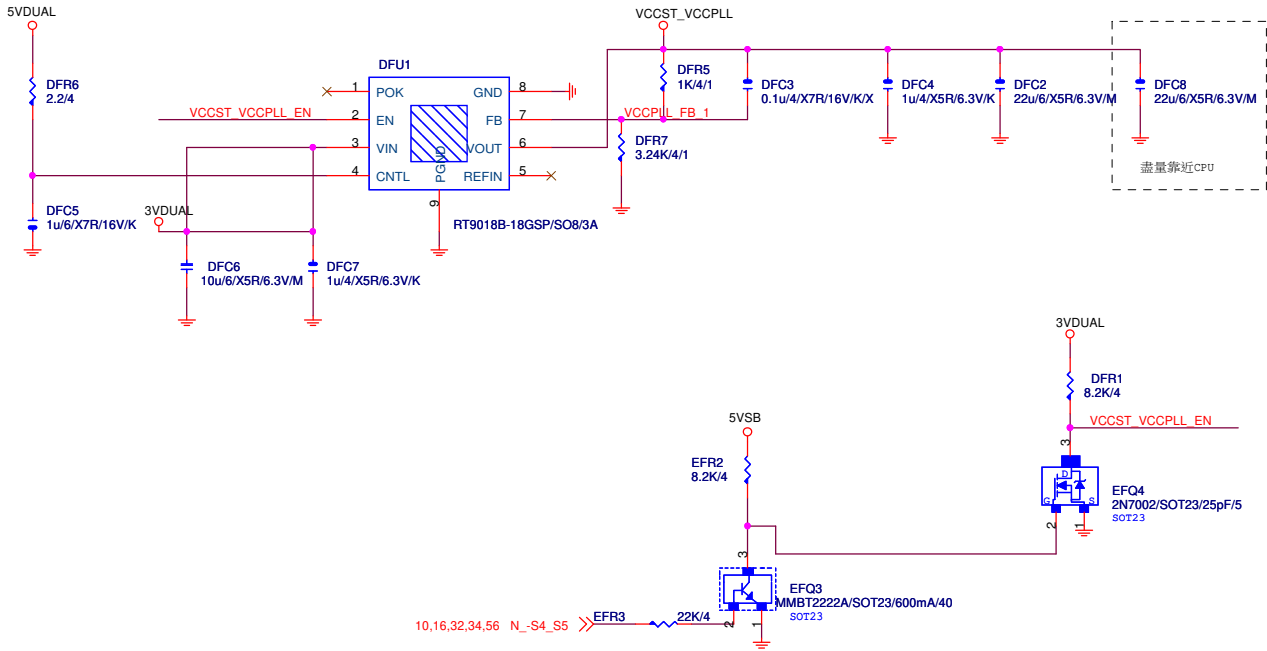
\* 大電容 x0



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Title			
RT8068A_VPP25 POWER			
Size	Document Number	Rev	
Custom	H510M H	1.0	
Date:	Wednesday, January 06, 2021	Sheet	34 of 62

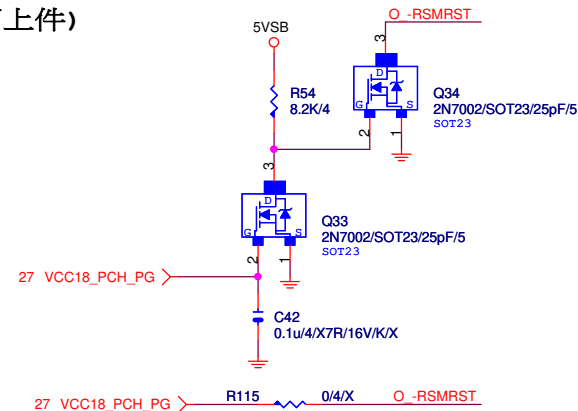
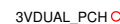
VCCST\_VCCPLL 替換原先MOS開關線路



16 5VAUX SW



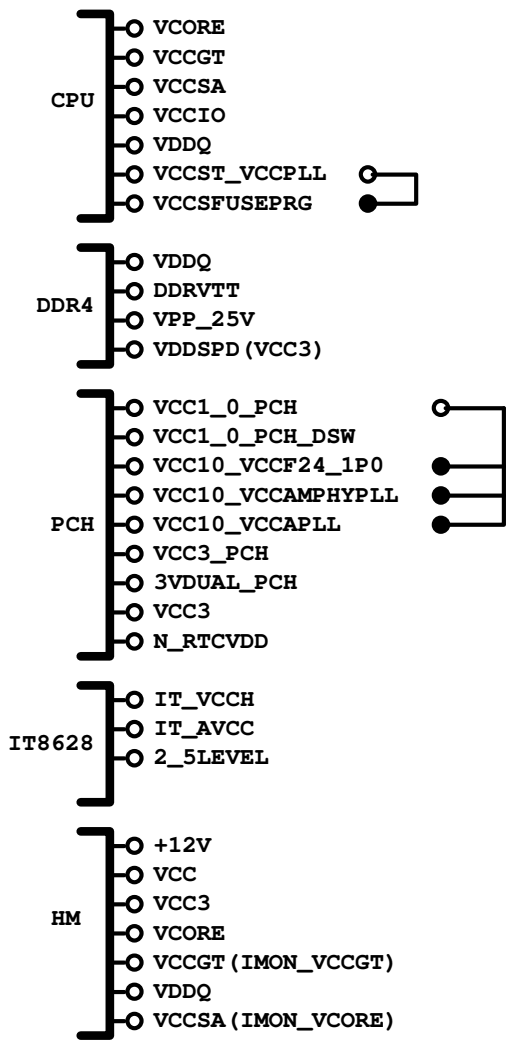
## 3VDUAL\_PCH



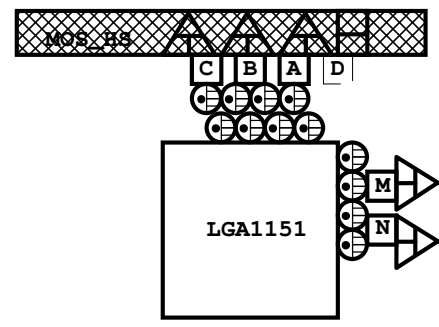
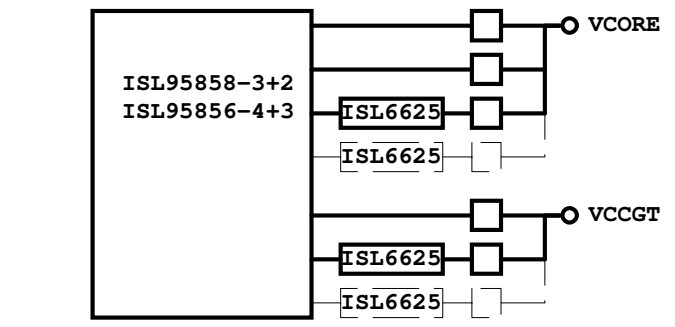
## Gigabyte Technology

Title			
<b>DISCRETE POWER</b>			
Size	Document Number		Rev
Custom	<b>H510M H</b>		<b>1.0</b>
Date:	Wednesday, January 06, 2021	Sheet	36 of 62

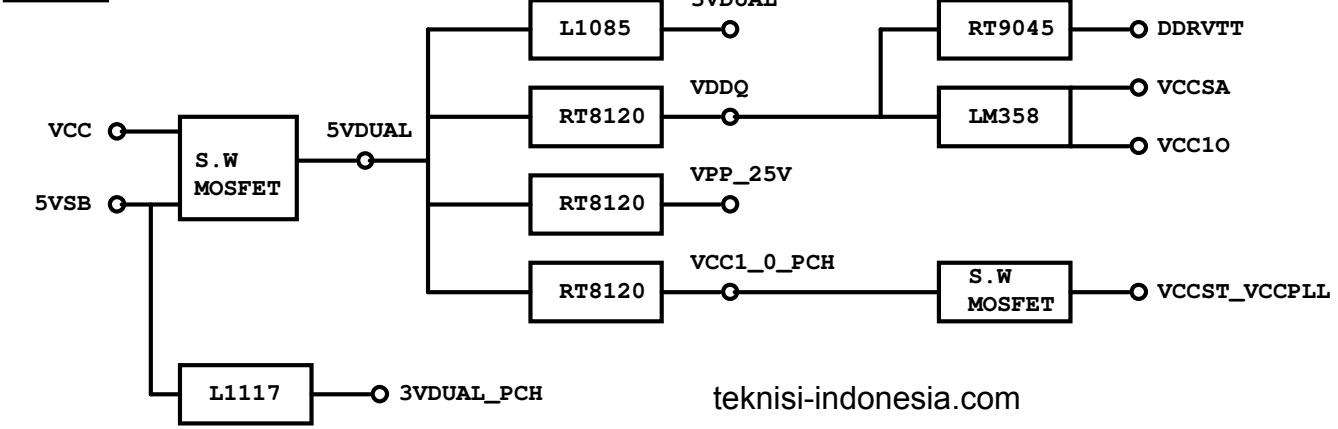
POWER BLOCK MAP



VCORE/VCCGT

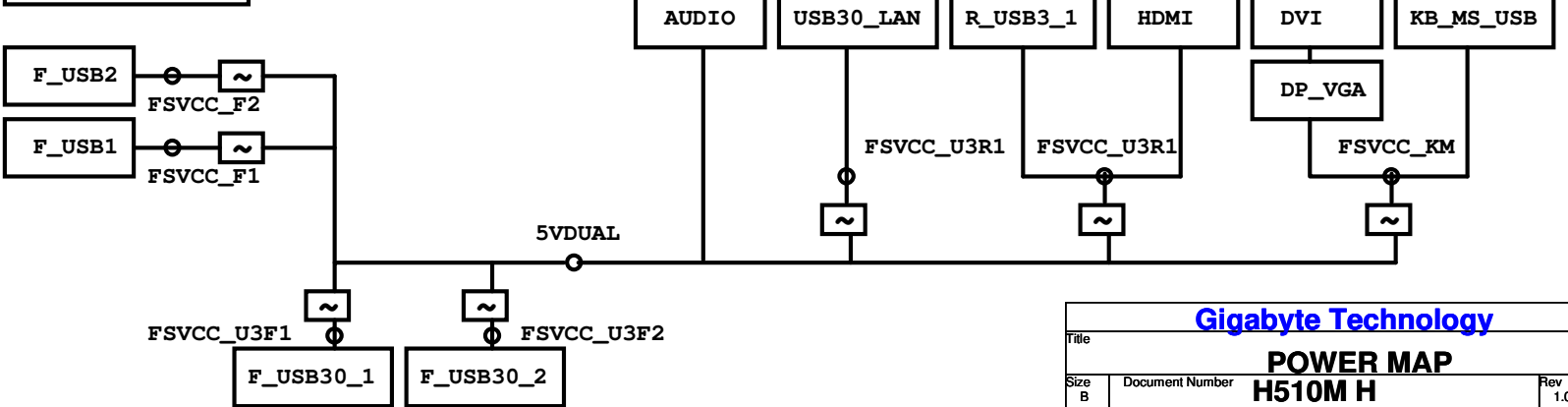


POWER



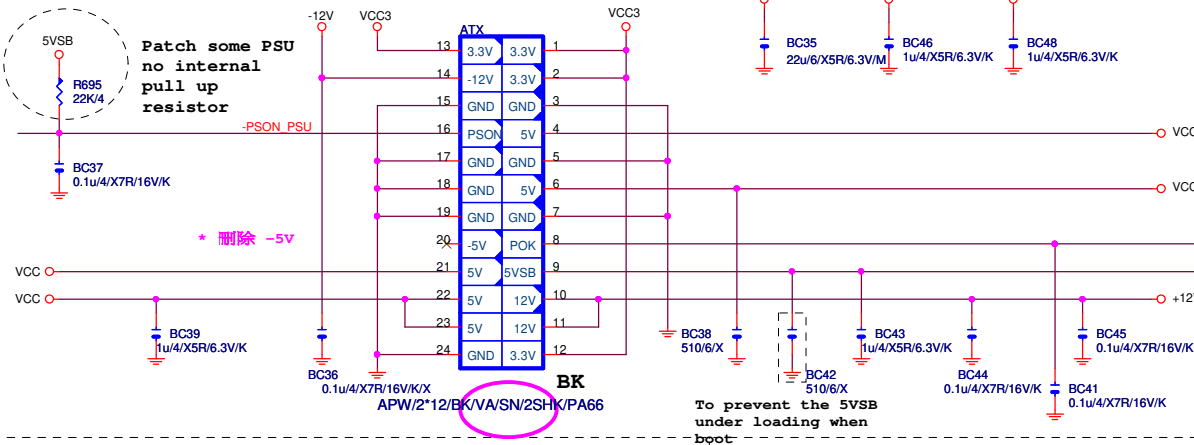
teknisi-indonesia.com

FUSE POWER F/R



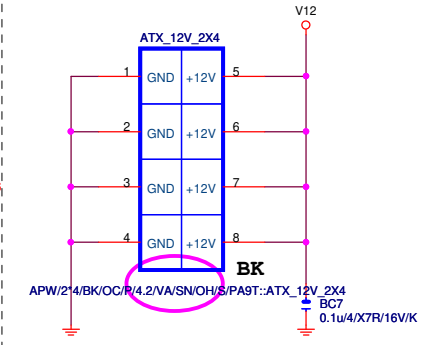
## ATXX24 POWER CONNECTOR

2x12 (空心Pin)  
FOOTPRINT: ATXPWR\_24-6

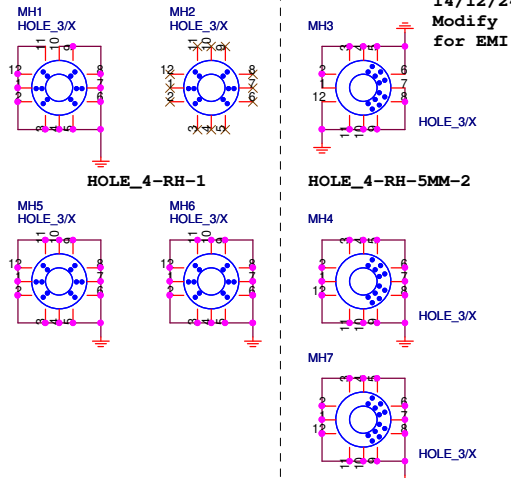


## ATXX4 POWER CONNECTOR

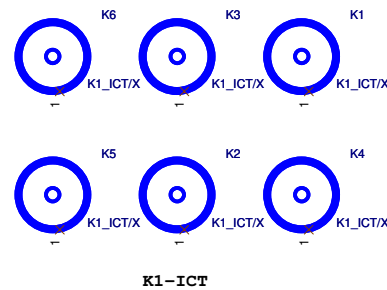
2x4 (實心Pin)  
FOOTPRINT: ATXPW2X4-SOLID



## 螺絲孔



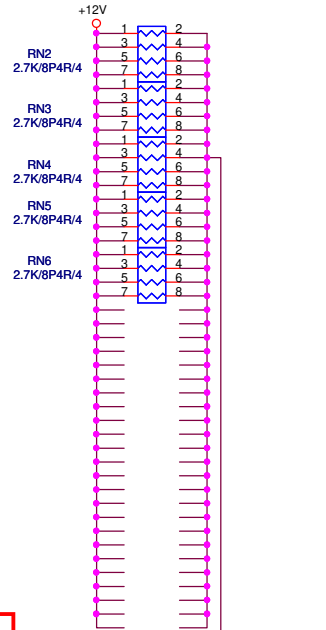
## 固定孔/光學點



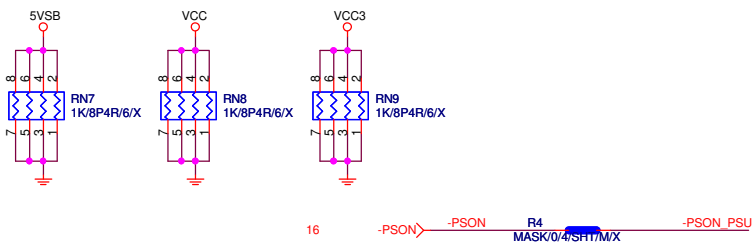
## +12V DUMMY LOAD

【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



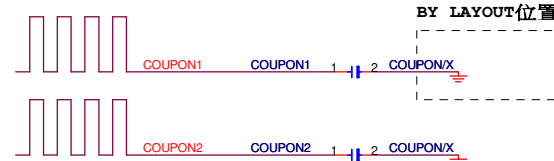
## DUMMY LOAD



## -PROHOT



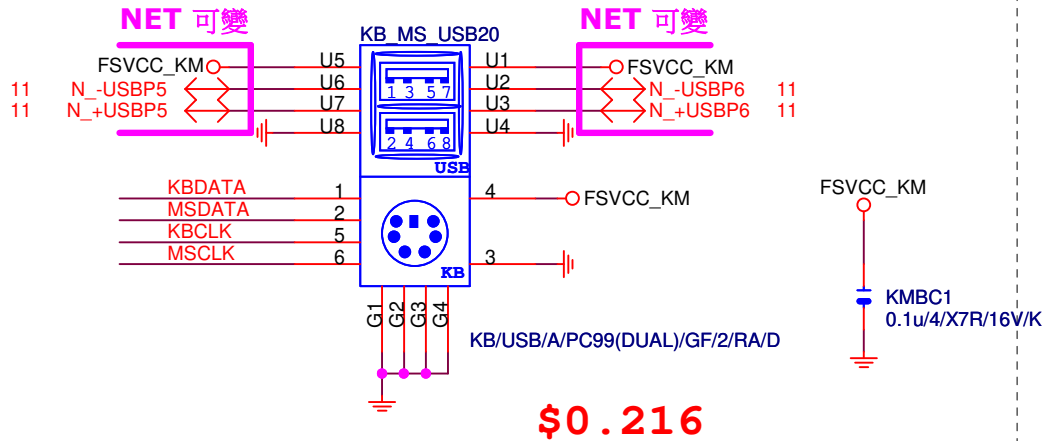
## COUPON



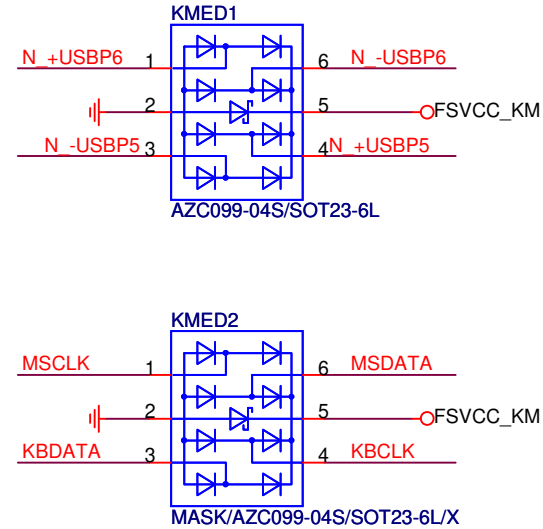
Gigabyte Technology

Title	ATX POWER CONNECTOR		
Size	Document Number	H510M H	
Custom		Rev 1.0	
Date:	Wednesday, January 06, 2021	Sheet 38	of 62

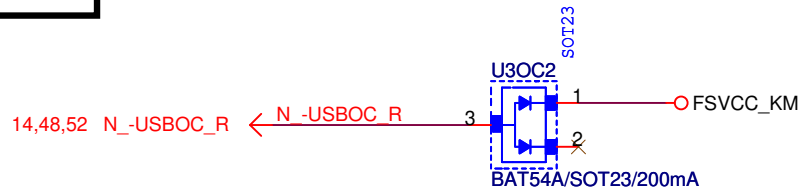
# KB\_MS\_USB



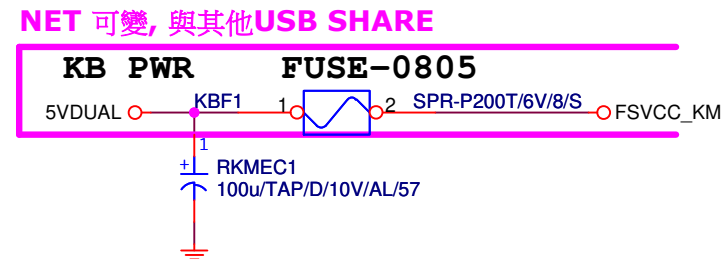
# ESD



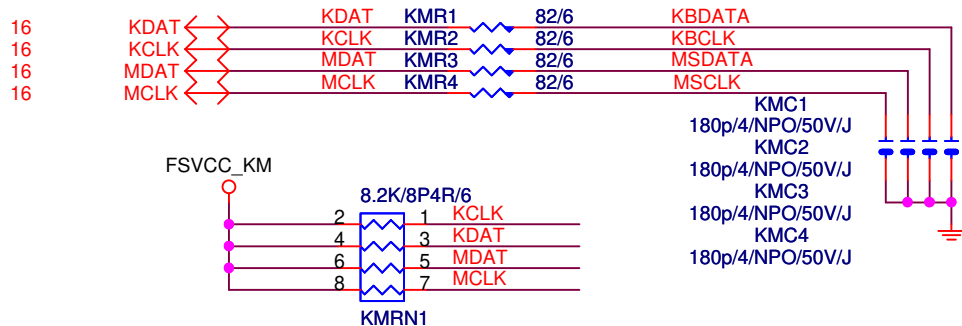
# USB OC PROTECT



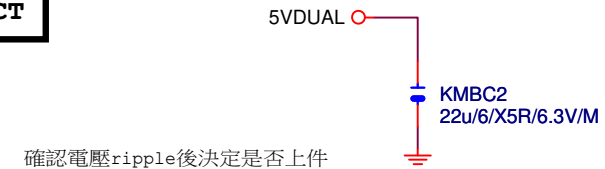
# KB\_MS\_USB PWR



# KB\_MS\_USB DAMPING/PU



# USB OC PROTECT



Gigabyte Technology

Title

KB\_MS

Size

Document Number

H510M H

Rev

1.0

Date:

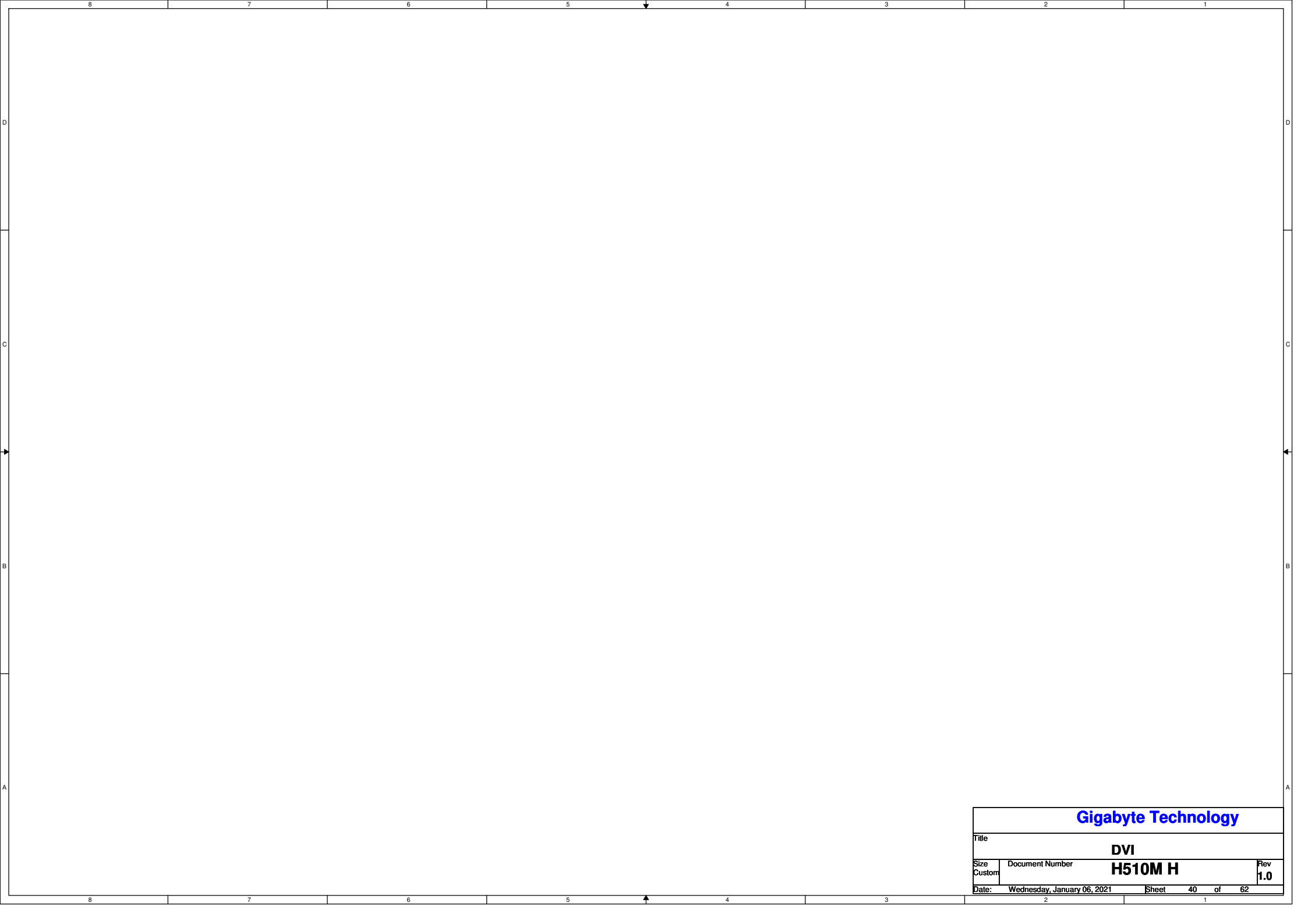
Wednesday, January 06, 2021

Sheet

39

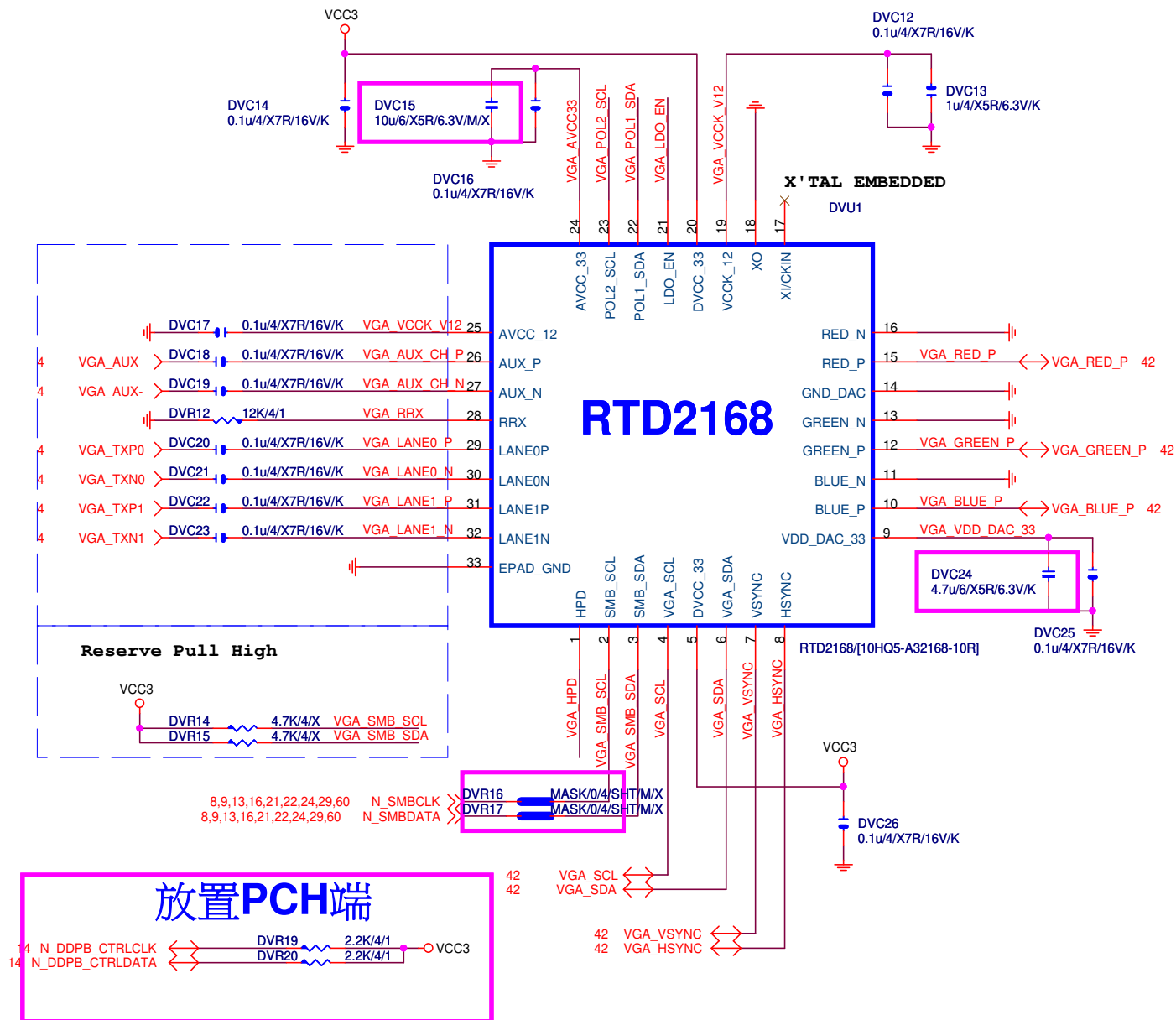
of

62



Gigabyte Technology			
Title			
DVI			
Size Custom	Document Number	H510M H	Rev 1.0
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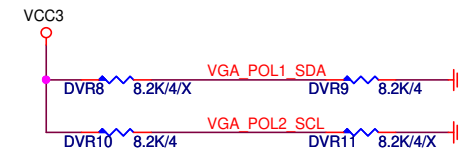




## POWER

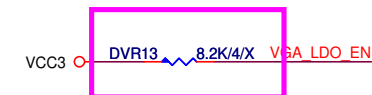


Power on latch



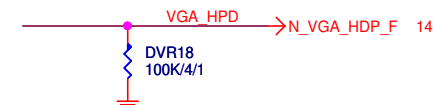
		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	<b>ROM ONLY MODE</b>	<b>EEPROM MODE</b>

### Embedded LDO

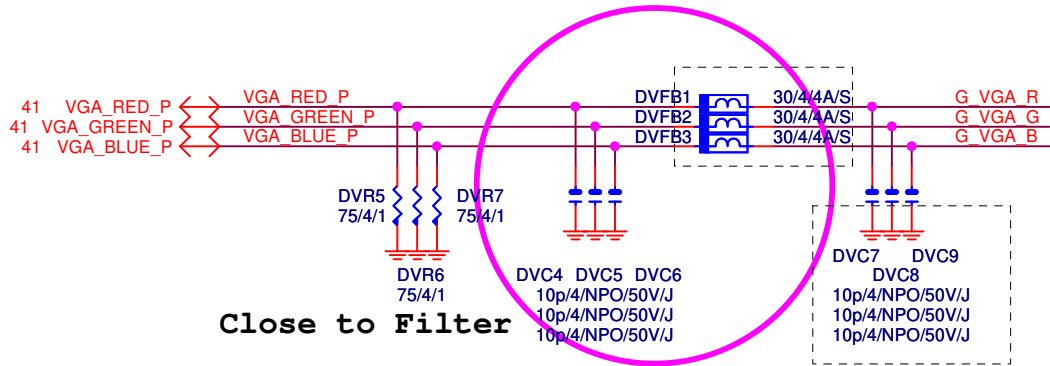
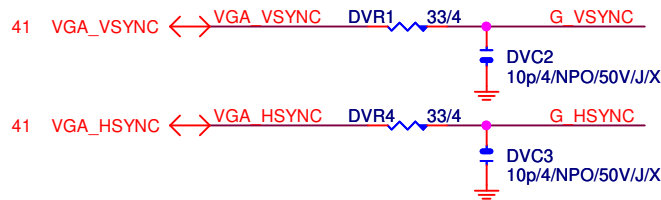
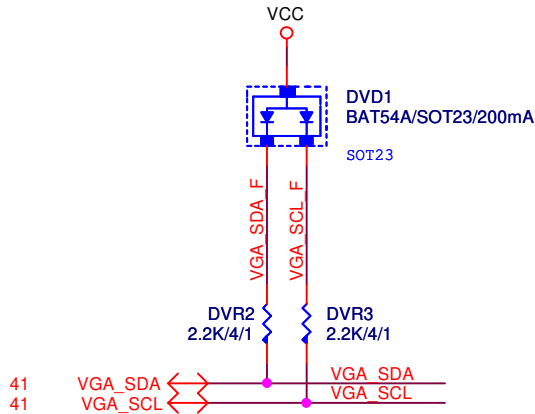


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

## DP HPD



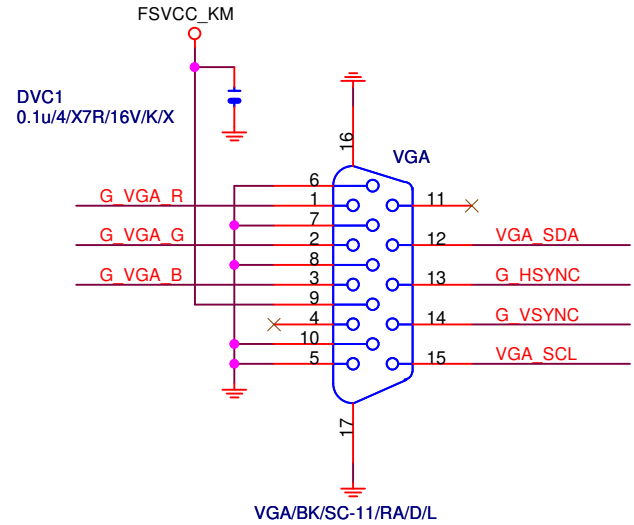
# VGA SIGNAL R2.0



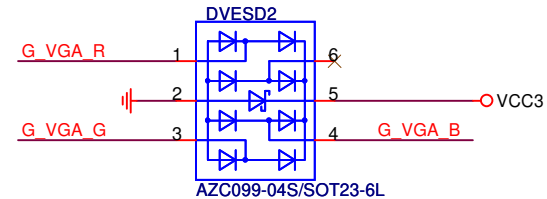
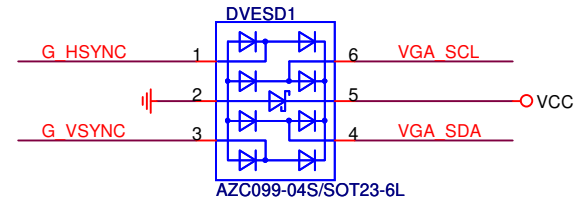
Close to Filter

FOR EMI

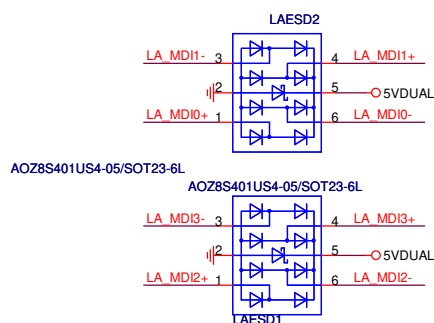
# VGA CONN.



# VGA ESD



Gigabyte Technology		
DP-VGA RTD2168		
Title	Document Number	Rev
Size	H510M H	1.0
Custom		
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(CLOSE LAU1 PIN22, 30, 3, 8)

PIN22  
LABC2  
1u4/X5R/6.3V/K

PIN30  
LABC9  
0.1u4/X7R/16V/K

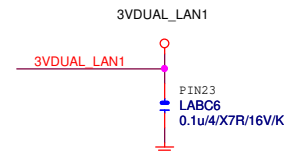
PIN3  
LABC3  
0.1u4/X7R/16V/K

PIN8  
LABC8  
0.1u4/X7R/16V/K

LA\_DVDD10

```
LABC2:1U CLOSE PIN22[REALTEK REQ]
```

note: lan power 連接及電流



(CLOSE LAU1 PIN23)

(CLOSE LAU1 PIN:11,32)

LA\_VDD33

P1N1

LABC18 0.1u/4/X7R/16V/K

LABC27 4.7u/6/X5R/6.3V/K

P1N3Z

LABC14 0.1u/4/X7R/16V/K

LABC20 4.7u/6/X5R/6.3V/K

PWR SURGE

LABC18,27:CLOSE PIN11 [REALTEK SURGE]

LABC14, 20:CLOSE PIN32 [REALTEK SURGE]

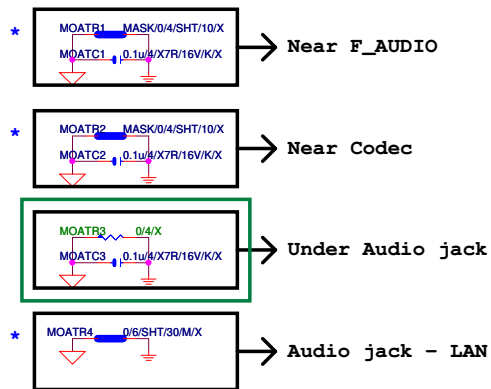
[illegible]

<p align="center"><b><i>Gigabyte Technology</i></b>  <b><i>Realtek RTL8111G</i></b></p>			
Title			
Size Custom	Document Number		Rev
	H510M H		1.0
Date:	Wednesday, January 06, 2021	Sheet	43 of 62



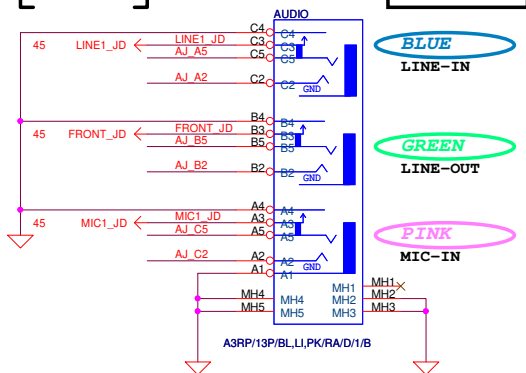
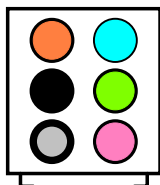


Rev 6.0

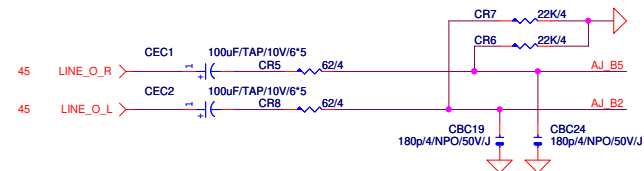


\*量産前,MOATR1/MOATR2/MOATR4 ....0ohm改short pad

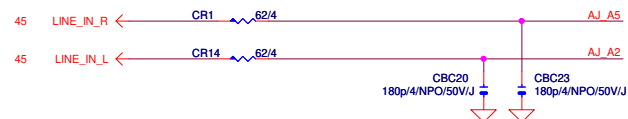
# AZALIA JACK



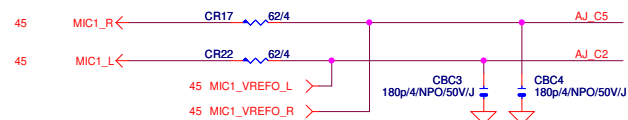
## LINE-OUT



## LINE-IN



## MIC-IN

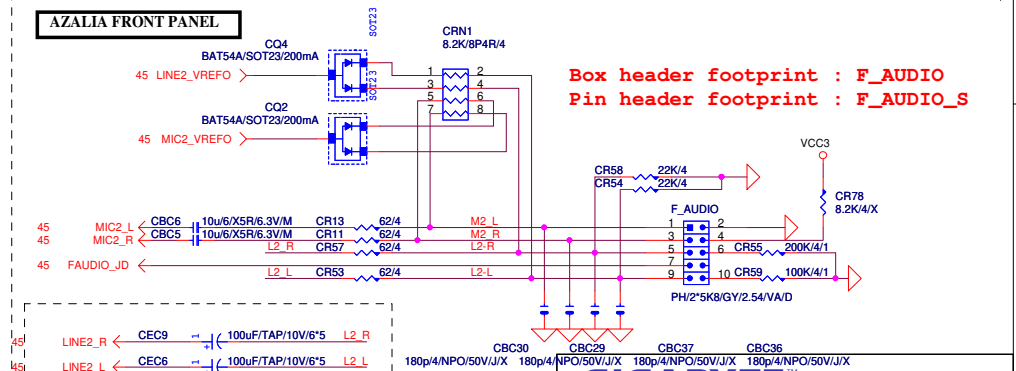


## SURROUND

## CEN/LFE

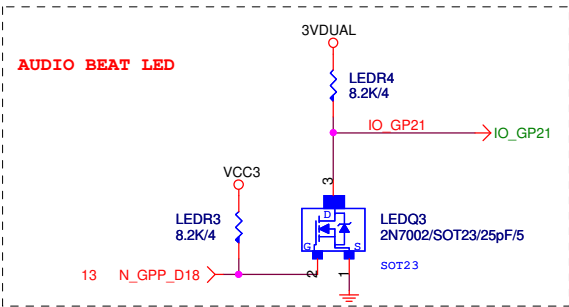
## SURR BACK

## AZALIA FRONT PANEL



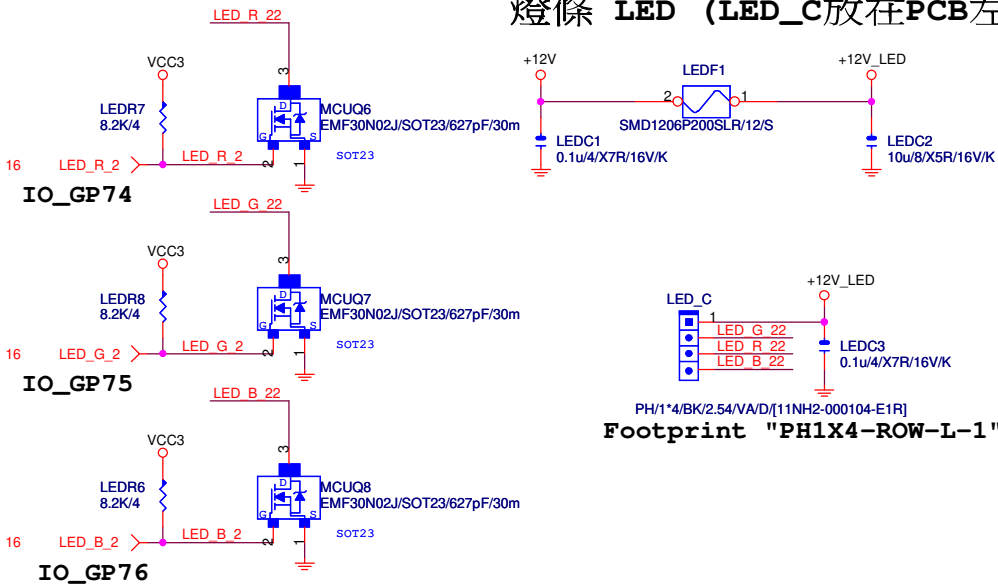
GIGABYTE

Title		AUDIO JACK	
Size	Document Number	H510M H	Rev 1.0
Date:	Wednesday, January 06, 2021	Sheet 46	of 62



## 第二區 LED CONTROL

燈條 LED (LED\_C放在PCB左邊板邊位置)



PH/1\*4/BK/2.54/VA/D[11NH2-000104-E1R]  
Footprint "PH1X4-ROW-L-1"

# GIGABYTE™

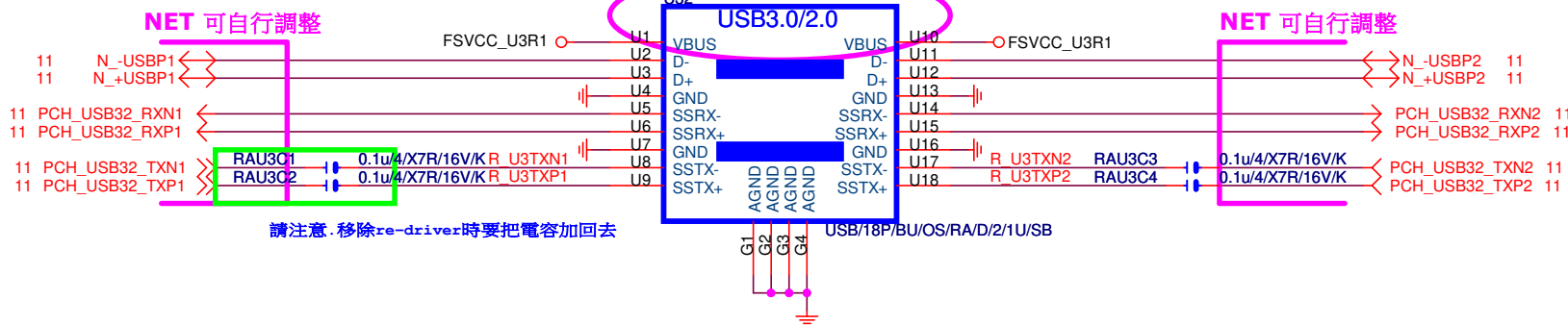
## Amient Single LED

Size	Document Number	Rev
Custom	<b>H510M H</b>	<b>1.0</b>

Date: Wednesday, January 06, 2021 Sheet 47 of 60

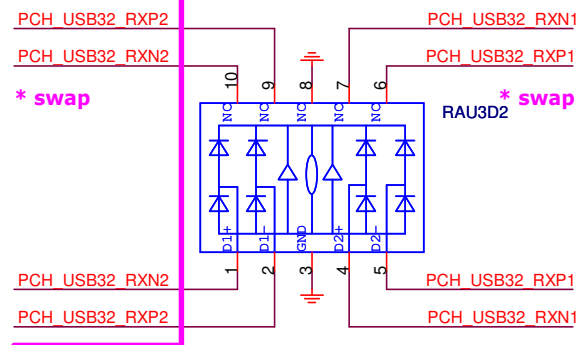
Rev: 0.7

ESD 可自行SWAP PIN ,CONN端 NET 名稱 不可



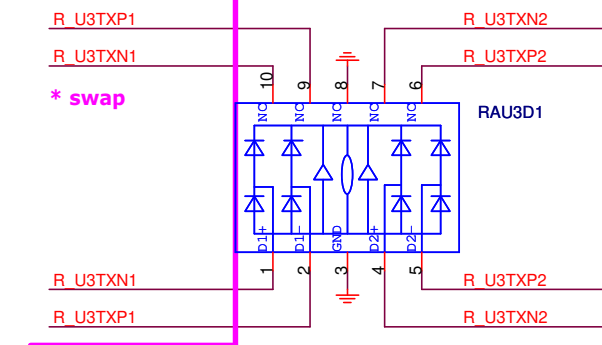
ESD

NET 可自行調整



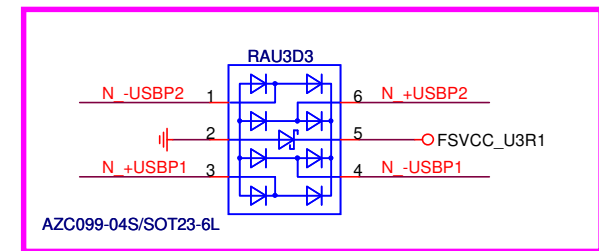
AZ1045-04F/MSOP10[10DE2-140174-10R\_10DE2-360148-10R]

NET 可自行調整



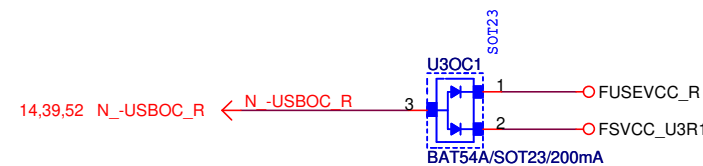
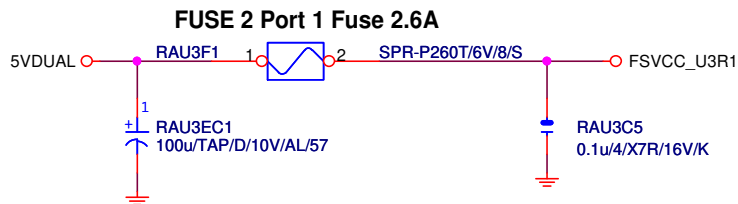
AZ1045-04F/MSOP10[10DE2-140174-10R\_10DE2-360148-10R]

NET 可自行調整



AZC099-04S/SOT23-6L

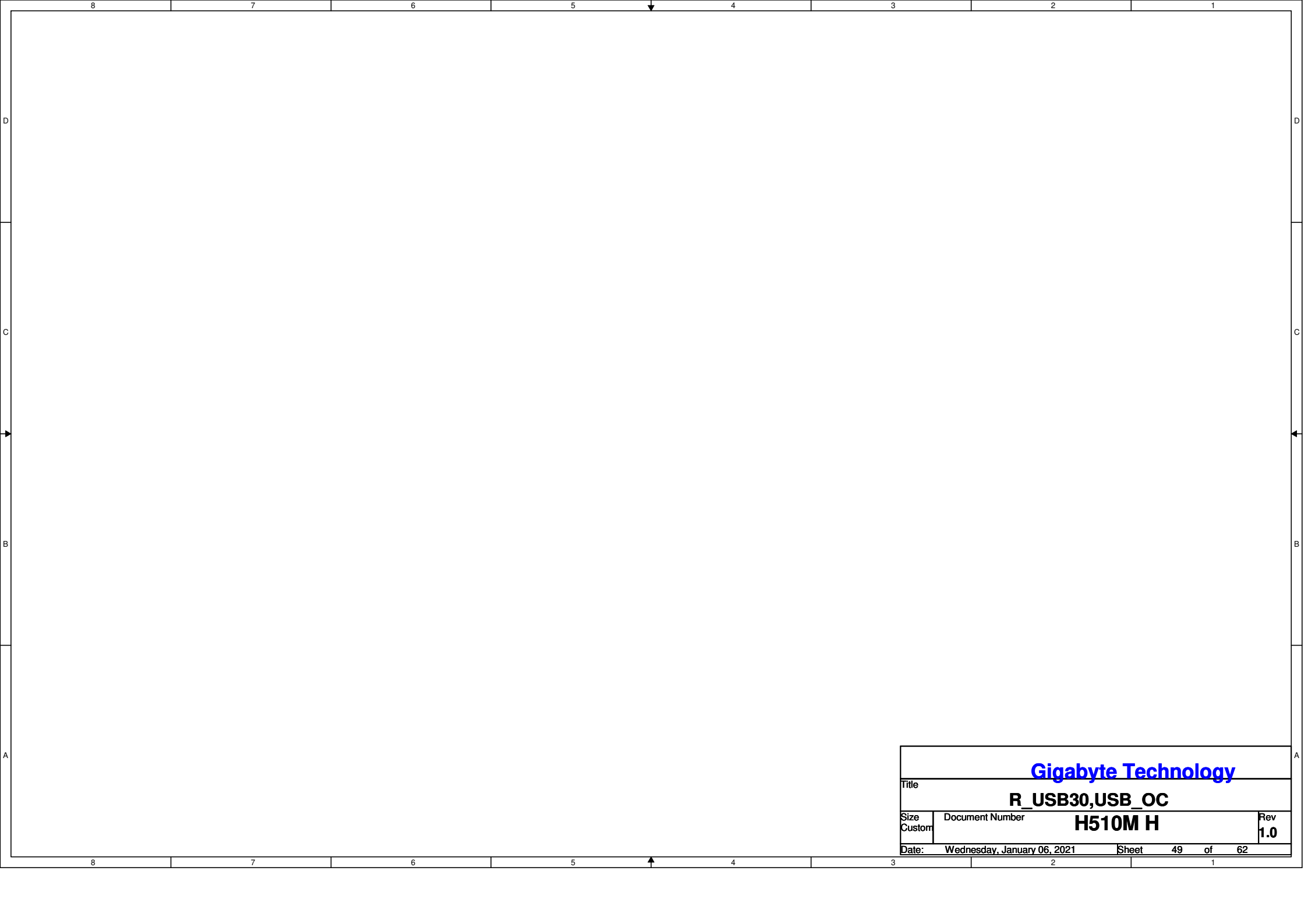
FUSE



Gigabyte Technology

Title					Rev 1.0
R_USB30,USB_OC					
Size Custom	Document Number				H510M H
Date: Wednesday, January 06, 2021		Sheet 48 of 62			



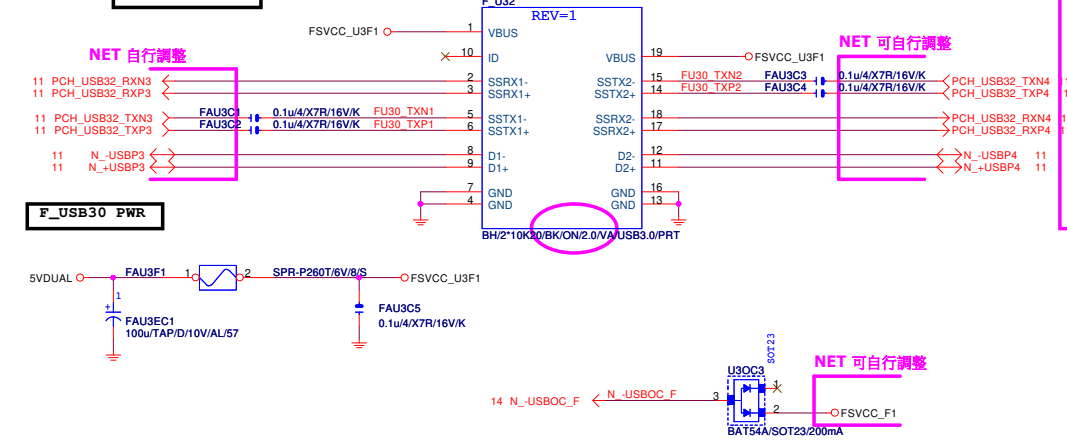


Gigabyte Technology			
Title			
R_USB30,USB_OC			
Size	Document Number		Rev
Custom	H510M H		1.0
Date:	Wednesday, January 06, 2021	Sheet	49 of 62

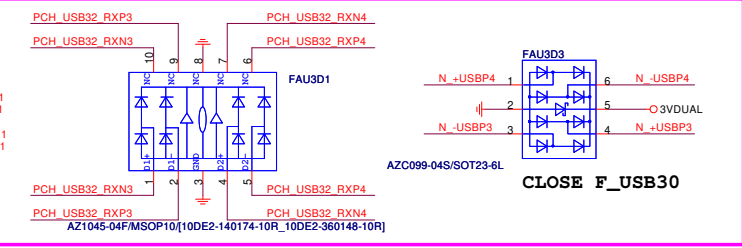




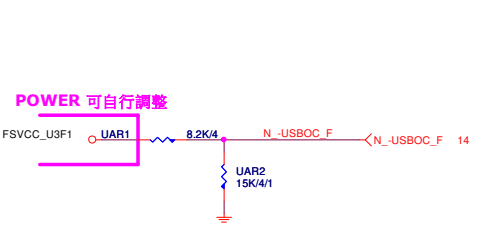
Front USB3.0



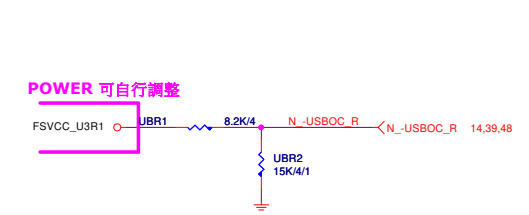
NET 可自行調整



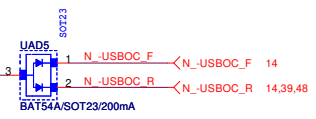
-USBOC\_F



-USBOC\_R



\* 接 PCH  
N\_GPP\_G7(SMI) &  
PCH PU 3Vdual

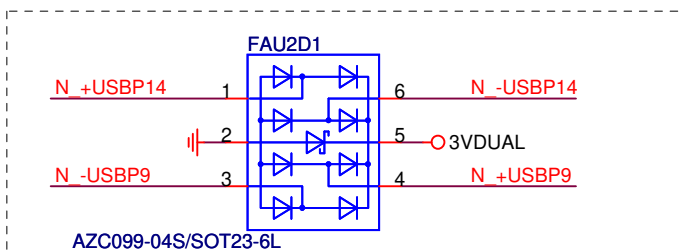
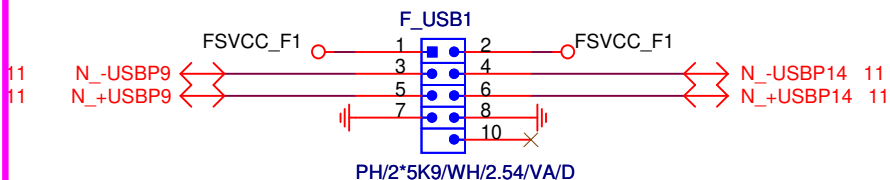


Rev: 0.7

FRONT USB1

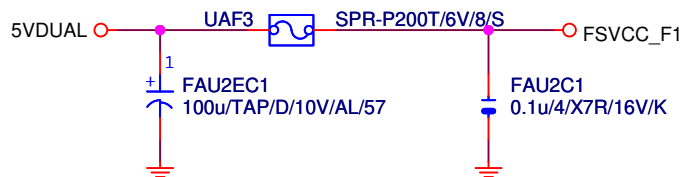
NET 可變

FUSB2X5-HS



Close to connector

FUSE 2 Port 1 Fuse 2A



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F\_USB 2.0 OC SIGNAL

Gigabyte Technology

Title

USB2.0

Size  
A

Document Number

H510M H

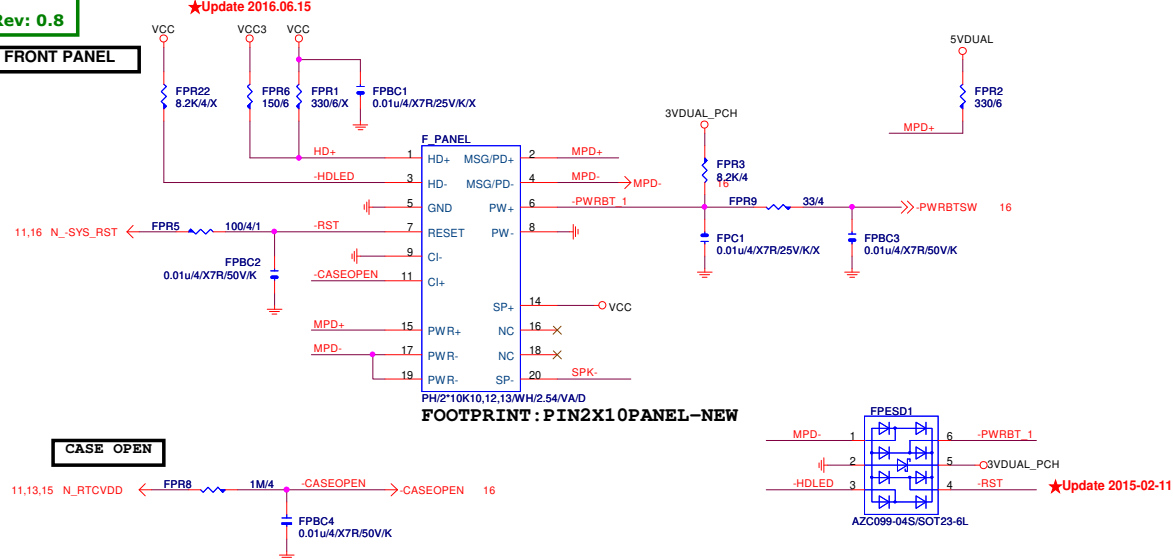
Rev  
1.0

Date: Wednesday, January 06, 2021

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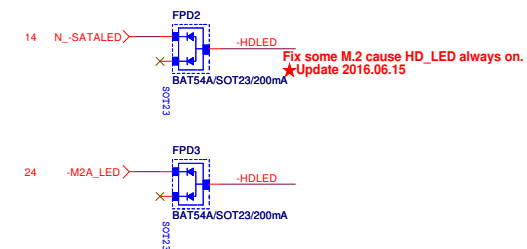
**Rev: 0.8**

## FRONT PANEL

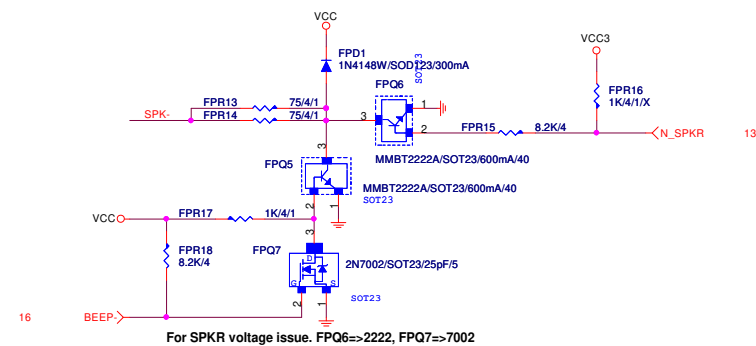


## FRONT PANEL SHORT

**SATA/M.2 LED**

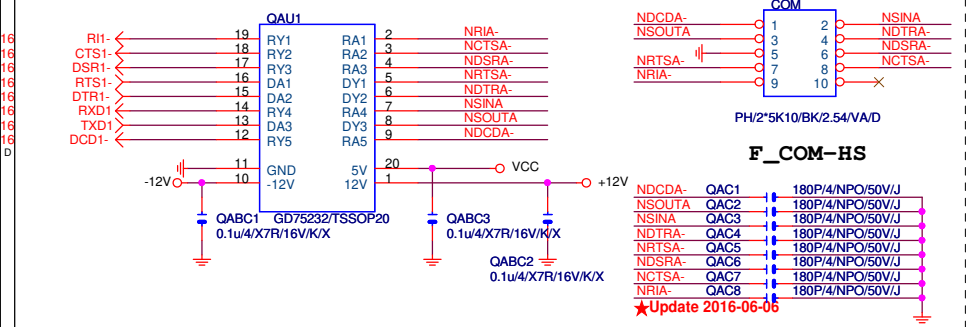


## SPKR



COM PORT

Rev: 0.7

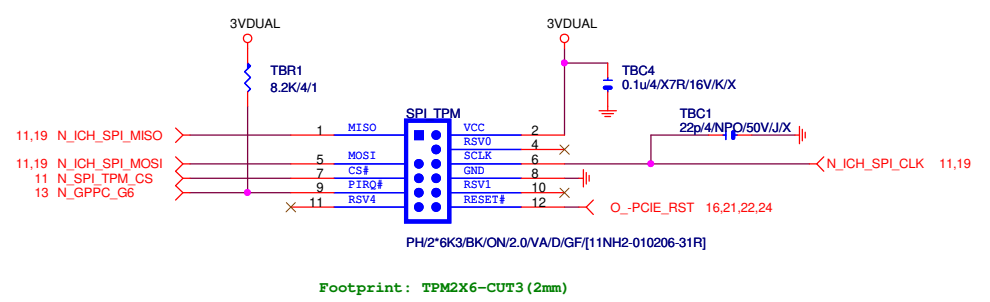


LPT PORT

COM RI

N/A

TPM CONNECT



Footprint: TPM2X6-CUT3 (2mm)

Gigabyte Technology		
Title		
FP,F_USB,USB PWR,BZ		
Size	Document Number	Rev
Custom	H510M H	1.0
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## CLOSE SIO

EMIC1  
100p/4/NPO/50V/J/X

10, 6, 32, 33 N\_SLP\_S3 ←

EMIC2  
100p/4/NPO/50V/J/X

10, 16, 32, 34, 35 N\_S4\_S5 ←

## CLOSE PCH

EMIC4  
100p/4/NPO/50V/J/X

4, 1) N\_CPUPWROK ←

## CLOSE NR47

VCC3

EMIC3  
0.1u/4/X7R/16V/K**GIGABYTE™**

Title

**EMI/ESD**Size  
A

Document Number

**H510M H**

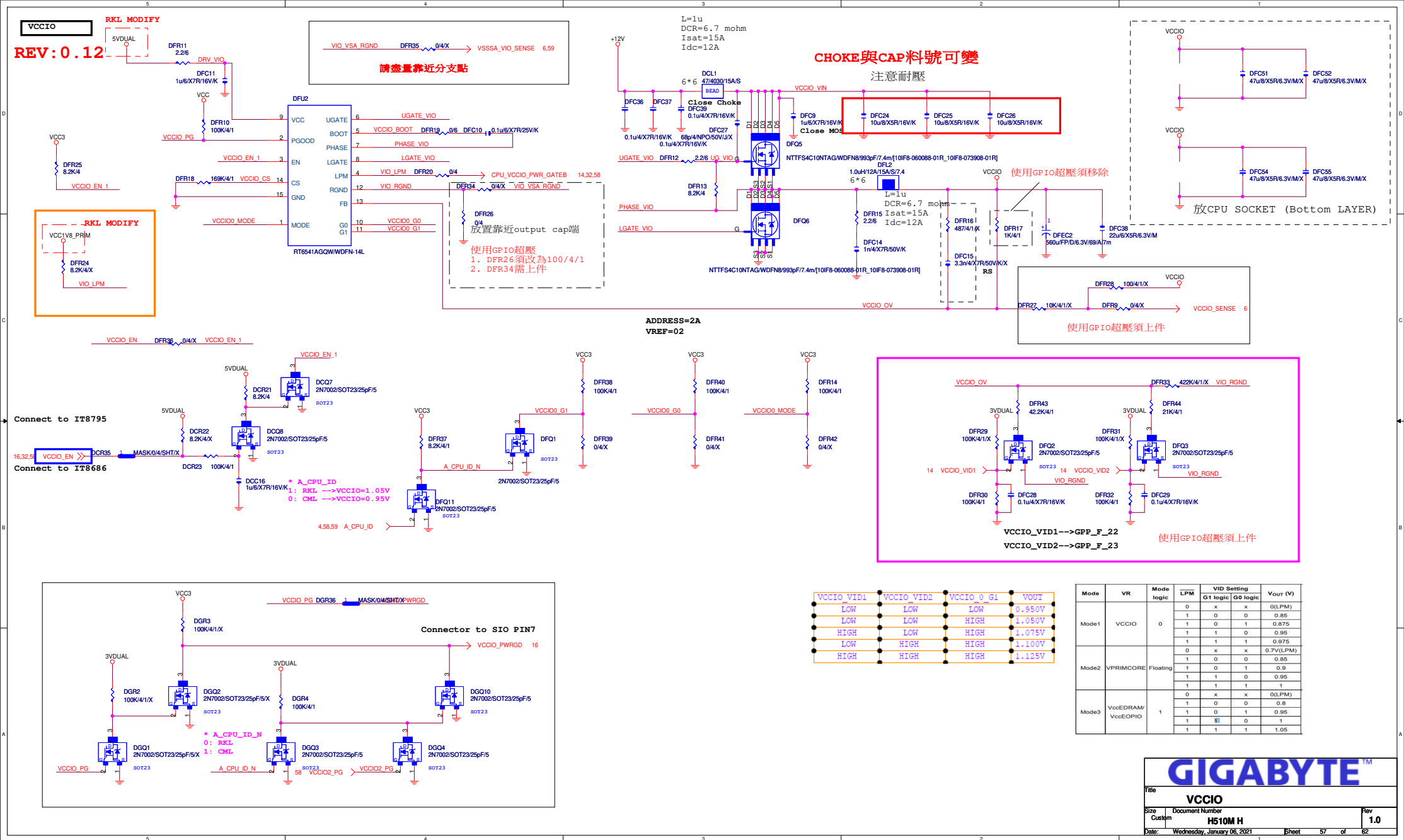
Rev

**1.0**

Date: Wednesday, January 06, 2021

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VCCIO2

RKL MODIFY

REV: 0.11

VCC3

VCC1V8\_P1M

有使用CPU POWER時DCR22不上件

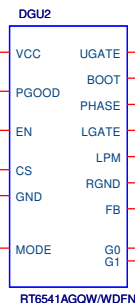
Connect to IT8795

Connect to IT8686

Connect to PCH

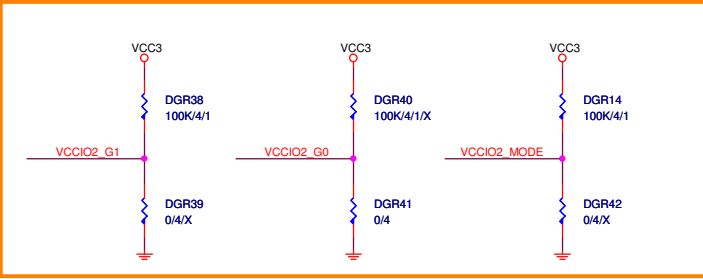
\* CPU\_ID  
1: RKL -->VCCIO=0.95V  
0: CML -->VCCIO=0V

4,57,59 A\_CPU\_ID > DGR37 1 MASK/0/4/SHT/X



從output CAP端拉回

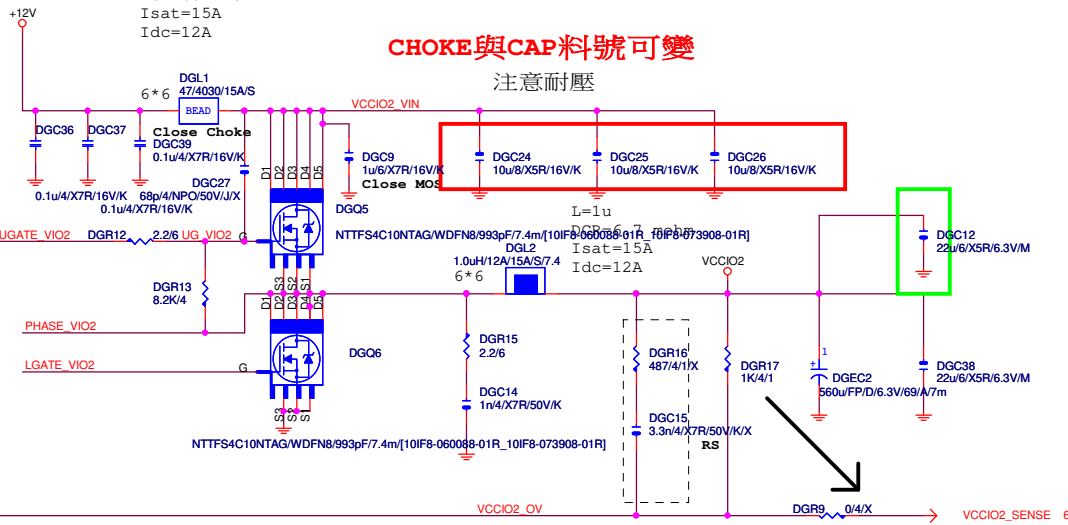
ADDRESS=24  
VREF=02



L=1u  
DCR=6.7 mohm  
Isat=15A  
Idc=12A

CHOKE與CAP料號可變

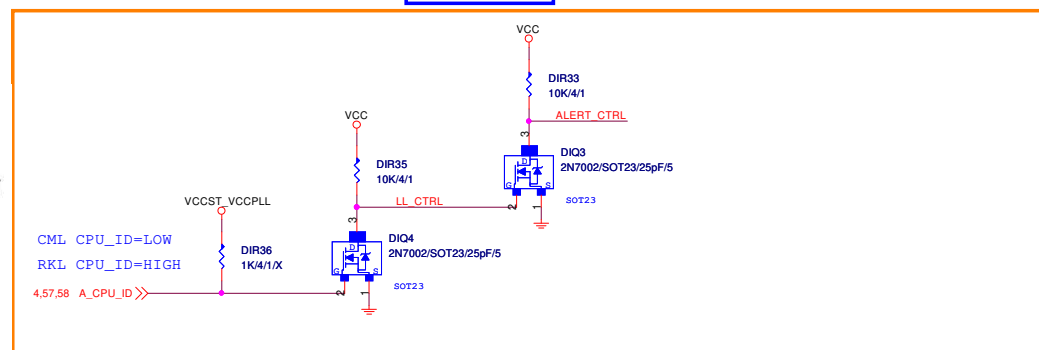
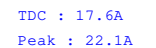
注意耐壓



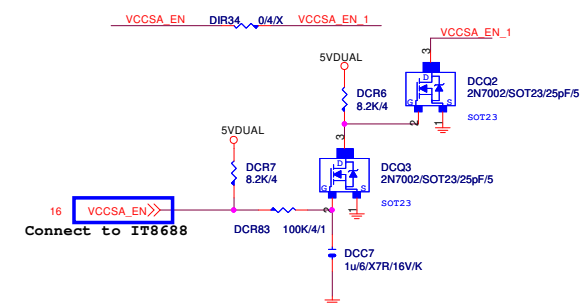
Remote sense請從最重的負載端點拉回

GIGABYTE<sup>TM</sup>

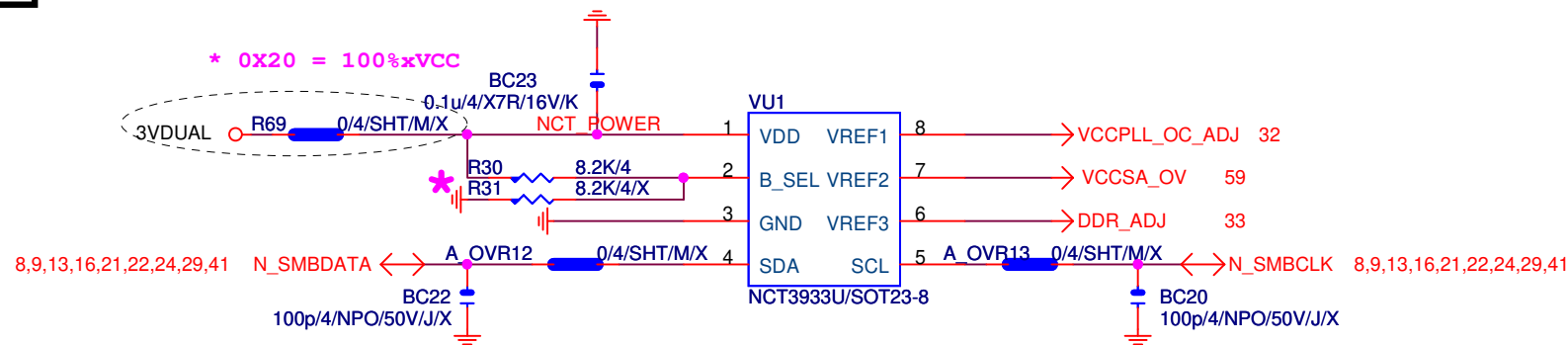
Title			VCCIO2
Size	Document Number	Rev	
Custom	H510M H	1.0	
Date:	Wednesday, January 06, 2021	Sheet	58 of 62



- When CPU\_ID = 0 (CML-S CPU), set DC load line to 0 Ohm and disconnect VCCSA SVID Alert# from common (VCCCORE/VCCGT) SVID Alert# bus. A bypass feature (0 ohm) resistor should be provided around the disconnect circuit.
- When CPU\_ID = 1 (RKL-S CPU), set DC load line to 10.3mOhm and connect VCCSA SVID Alert# to common SVID Alert# bus



OVER VOLTAGE



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

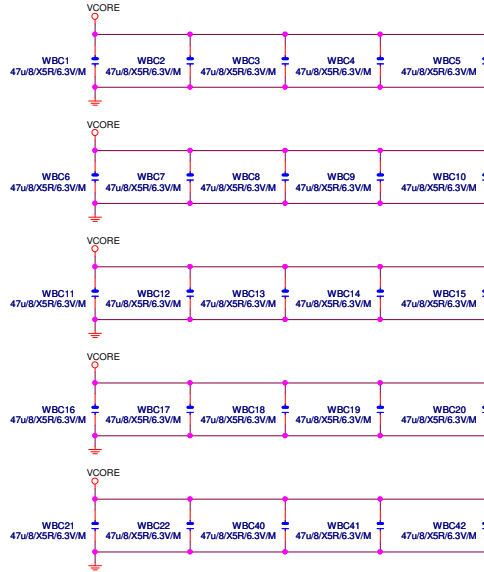
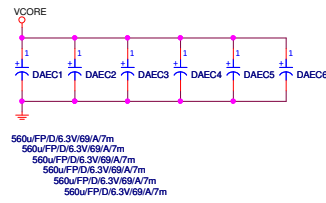
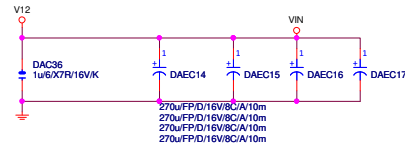
Table1. Recommended Slave Address Setting

NCT3933	
VREF1	VCCPLL_OC
VREF2	VCCSA
VREF3	VDDQ

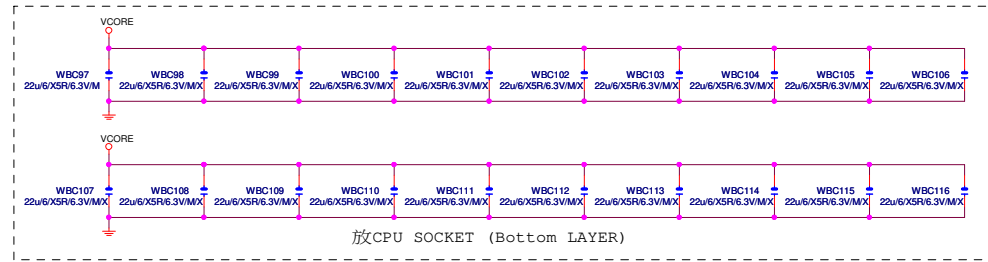
Title		
NCP3933		
Size	Document Number	Rev
A	H510M H	1.0
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VIN CAP 270u\*4PCS

VCORE CAP 560u\*6PCS  
22u\*20PCS

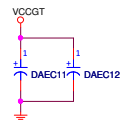


放CPU SOCKET (TOP LAYER)

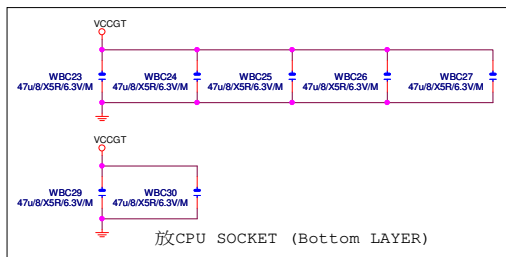


放CPU SOCKET (Bottom LAYER)

VCCGT CAP 560u\*2PCS  
22u\*4PCS



560uF/16V/8C/A/10m  
22uF/6.3V/69A/7m

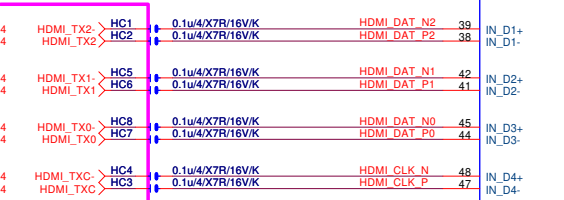


放CPU SOCKET (Bottom LAYER)

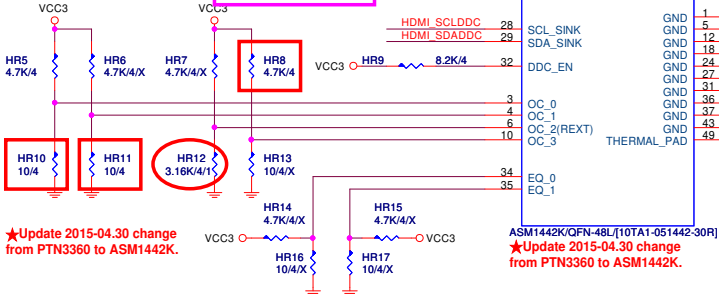
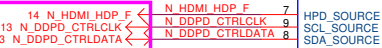
Title		
CPU CAP.		
Size	Document Number	Rev
Customer	#1510MH	1.0
Date:	Wednesday, January 05, 2021	Sheet 61 of 62

HDMI LEVEL SHIFT

NET 可變



Port 自行調整

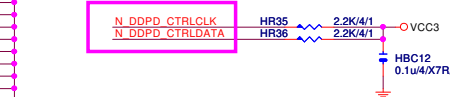


★Update 2015-04.30 change from PTN3360 to ASM1442K.

★Update 2015-04.30 change from PTN3360 to ASM1442K.

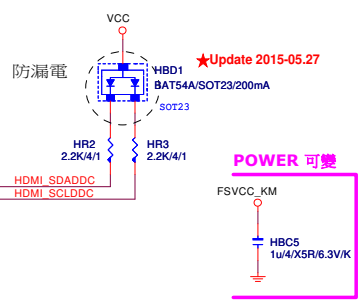
PTN3360:PIN 4/10/34/35 NC PIN, 都不上值; 只上HR12:10K  
ASM1442:紅色框要上, HR12:3.16K

Port 自行調整



【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail  
原因: 因目前的HDMI訊號過長, 造成RISING TIME過慢, 而會壓到eye diagram  
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



POWER 可變

